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**Cortex®-M0+ based 32-Bit General-Purpose Microcontroller**

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DS Rev. 1.00

**Features****Core**

- Arm® Cortex®-M0+ core
- Up to 48 MHz clock speed

**Memory**

- 256 KB code Flash memory with ECC
  - Read protection for security
- 32 KB SRAM

**Clock, Reset and Power Management**

- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Low Voltage Detection
  - Low Voltage Reset (LVR)
  - Low Voltage Indicator (LVI)
- Power management for power consumption
  - RUN, SLEEP, DEEP-SLEEP modes
- Clock monitoring function for system clock

**Interrupt Management**

- Nested Vectored Interrupt Controller (NVIC) with 31 interrupt sources

**General-Purpose Input/Output**

- Up to 53 I/O pins
- 53 mappable on external interrupt vectors
- Strength input/output

**DMA Controller**

- Four channels of Direct Memory Access
- 8/16/32-bit data transfers
- Conjunction with 19 internal peripherals

**USB 2.0 Full Speed**

- Crystal-less with clock management unit
- 1024 bytes packet buffer memory SRAM
- Number of endpoints from 1 to 5 in addition to Endpoint 0

**Comparator**

- Two comparators

**ADC**

- One independent ADC block
- 16 analog input channels
- 7-bit prescaler
- 1 Msps conversion rate

**Timer**

- 16-bit timers: 6 channels
- 32-bit timers: 2 channels
- Timer operating modes
  - Timer/counter mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 12-bit prescaler

**Watchdog Timer**

- 24-bit down-count timer
- Reset and periodic interrupts
- Four dividers selectable

**Real Time Clock and Calendar**

## Communication Interfaces

- USART
  - Four Universal Synchronous Asynchronous Serial Receiver-Transceiver ports
- I2C
  - Three Inter-Integrated Circuit interface ports
- SPI
  - Two Serial Peripheral Interface ports

## CRC Calculation Unit

- CRC operating modes:
  - CRC-CCITT
  - CRC-16
  - Auto CRC/User-defined CRC
  - CRC and checksum

## Temperature Sensor

### Debug Interface

- Serial Wire Debug (SWD) interface

### Package

- 64-LQFP-1010 (0.50 mm pitch)
- 64-LQFP-1212 (0.65 mm pitch)
- 48-LQFP-0707 (0.50 mm pitch)
- 48-QFN-0505 (0.35 mm pitch)
- 40-QFN-0505 (0.40 mm pitch)
- 32-QFN-0505 (0.50 mm pitch)

### Operating Voltage

- 1.8 V to 5.5 V

### Operating Temperature

- Commercial grade (−40°C to 85°C)

## Product Selection Table

Table 1. Device Series Summary

Base Product	Part Number	Flash	SRAM	USART	SPI	I2C	USB	ADC	Timer	I/O Ports	Package
A31G336	A31G336RL	256 KB	32 KB	4	2	3	1	16	8	53	64-LQFP-1010
	A31G336RM	256 KB	32 KB	4	2	3	1	16	8	53	64-LQFP-1212
	A31G336CL	256 KB	32 KB	4	2	3	1	10	8	37	48-LQFP-0707
	A31G336CU	256 KB	32 KB	4	2	3	1	10	8	37	48-QFN-0505
	A31G336IU	256 KB	32 KB	3	1	3	1	9	8	29	40-QFN-0505
	A31G336KU	256 KB	32 KB	2	1	3	1	8	8	22	32-QFN-0505

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## 1. Introduction

This document provides an overview of the features supported by the device, including high-level information and brief explanations for each feature.

Refer to Table 3 for the list of features supported by the device.

## 2. Description

The A31G336 is a 32-bit microcontroller based on the energy efficient Arm Cortex-M0+ core, with up to 256 KB of code Flash memory with ECC, and 32 KB of SRAM. The A31G336 operates at voltage range of 1.8 V to 5.5 V, providing a highly flexible and cost-effective solution for many embedded control applications.

The A31G336 features a variety of peripherals, including 16-bit and 32-bit timers, Real timer and calendar, a 12-bit ADC, Comparator, CRC generator, as well as USB 2.0 Full Speed, USART, I2C, SPI, and DMA. In addition, this device is equipped with a POR, LVR, LVI, and an internal RC oscillator.

To further reduce power consumption, the A31G336 supports both SLEEP and DEEP-SLEEP modes.

### 2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for the A31G336.

**Table 2. A31G336 Memory Capacity**

Memory Capacity		Category
Flash	RAM	
256 KB	32 KB	A31G336

## 2.2 Device Overview

Table 3 summarizes and lists the features specific to the device while considering the largest package.

**Table 3. A31G336 Features**

Item		Description
Core	CPU	<ul style="list-style-type: none"> <li>• Max. operating frequency: 48 MHz</li> <li>• 32-bit Arm Cortex-M0+ CPU</li> <li>• Register settings in CPU:               <ul style="list-style-type: none"> <li>- General purpose register: 32-bit Thumb-2 instruction set</li> <li>- Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13</li> <li>- Link Register (LR): R14</li> <li>- Program Counter (PC): R15</li> </ul> </li> <li>• Data ordering format: Little-Endian</li> <li>• Von Neumann Architecture</li> <li>• AHB/APB</li> </ul>
	Interrupt Controller	<ul style="list-style-type: none"> <li>• NVIC (Nested-Vectored Interrupt Controller)</li> <li>• Up to 32 peripheral interrupts supported.</li> <li>• Assignable with four different priority levels</li> </ul>
Memory	Code Flash	<ul style="list-style-type: none"> <li>• Capacity: 256 KB</li> <li>• A high-capacity Code Flash memory built in</li> <li>• Max. 48 MHz Flash access speed               <ul style="list-style-type: none"> <li>- 0-wait: up to 20 MHz</li> <li>- 1-wait: up to 40 MHz</li> <li>- 2-wait: up to 48 MHz</li> </ul> </li> <li>• Erase unit: Page (512-byte), Sector (2048-byte), Bulk (256 KB, full-chip)</li> <li>• Program unit: Word (4-byte)</li> <li>• Read protection</li> <li>• Self-programming</li> <li>• CRC code generation and verification for the Flash memory</li> <li>• Endurance: 10,000 cycles</li> <li>• Lifetime: 10 years</li> <li>• ECC (1-bit correction and 2-bit detection)</li> </ul>
	Boot ROM	<ul style="list-style-type: none"> <li>• It initiates the microcontroller's boot mode by receiving an external input signal at the BOOT pin.</li> <li>• UART boot mode</li> <li>• In-system programming               <ul style="list-style-type: none"> <li>- Users can program the internal Flash memory by using an application board to write data to the memory.</li> </ul> </li> </ul>
	SRAM	<ul style="list-style-type: none"> <li>• Capacity: 32 KB</li> <li>• Usable as a program's work area</li> <li>• Part of the SRAM can be remapped into an interrupt vector area</li> </ul>

**Table 3. A31G336 Features (continued)**

Item	Description
Operating Frequency	<ul style="list-style-type: none"> <li>Up to 48 MHz</li> </ul>
Clock	<ul style="list-style-type: none"> <li>High speed Internal oscillator (HSI)               <ul style="list-style-type: none"> <li>32 MHz (<math>\pm 1.5\%</math> @ Ta = 0°C to +50°C)</li> <li>32 MHz (<math>\pm 3\%</math> @ Ta = -40°C to +85°C)</li> </ul> </li> <li>Low speed Internal oscillator (LSI)               <ul style="list-style-type: none"> <li>40 kHz (<math>\pm 15\%</math> @ Ta = -40°C to +85°C)</li> </ul> </li> <li>External Main Oscillator (HSE): 2 MHz to 16 MHz</li> <li>External Sub-Oscillator (LSE): 32.768 kHz</li> <li>Phase-locked loop (PLL): 48 MHz</li> </ul>
Clock Monitoring	<ul style="list-style-type: none"> <li>System fail-safe function by clock monitoring               <ul style="list-style-type: none"> <li>High frequency internal RC oscillator (HSI)</li> <li>External main oscillator (HSE)</li> <li>External sub oscillator (LSE)</li> <li>Main system clock (MCLK)</li> </ul> </li> </ul>
Operation Mode	<ul style="list-style-type: none"> <li>RUN mode</li> <li>SLEEP mode</li> <li>DEEP-SLEEP (STOP) mode</li> </ul>
Reset	<ul style="list-style-type: none"> <li>nRESET pin reset</li> <li>Core reset</li> <li>Software reset</li> <li>POR (Power-On Reset)</li> <li>LVR (Low-Voltage Reset)</li> <li>WDTR (Watchdog Timer Reset)</li> <li>MON (Clock monitoring reset)</li> </ul>
VDC	<ul style="list-style-type: none"> <li>Low-dropout (LDO) regulator built in for low-voltage operation</li> </ul>
POR	<ul style="list-style-type: none"> <li>The POR generator detects an internal 1.4 V and generates a reset signal</li> </ul>
LVI	<ul style="list-style-type: none"> <li>13 low-voltage detection levels</li> <li>Supports interrupts</li> <li>Supports wake-up from SLEEP mode and DEEP SLEEP modes</li> </ul>
Wake-up	<ul style="list-style-type: none"> <li>Wake-up by an external interrupt (GPIO) pin</li> <li>Wake-up by a Real Time Clock/Calendar (RTCC)</li> <li>Wake-up by a Watchdog Timer (WDT)</li> <li>Wake-up by a Low-Voltage Indicator (LVI)</li> <li>Wake-up by a I2C</li> <li>Wake-up by a USART</li> <li>Wake-up by a T20</li> <li>Wake-up by a comparator</li> <li>Wake-up by a USB</li> </ul>

**Table 3. A31G336 Features (continued)**

Item	Description
Wake-Up Timer (WUT)	<ul style="list-style-type: none"> <li>• 16-bit down-count timer</li> <li>• Underflow interrupt</li> <li>• Stabilization time upon wake-up from deep sleep mode</li> </ul>
General-Purpose I/O (GPIO)	<ul style="list-style-type: none"> <li>• Input/Output (I/O) port for general purpose</li> <li>• 64-LQFP-1010               <ul style="list-style-type: none"> <li>- I/O pins: 53</li> </ul> </li> <li>• 64-LQFP-1212               <ul style="list-style-type: none"> <li>- I/O pins: 53</li> </ul> </li> <li>• 48-LQFP-0707               <ul style="list-style-type: none"> <li>- I/O pins: 37</li> </ul> </li> <li>• 48-QFN-0505               <ul style="list-style-type: none"> <li>- I/O pins: 37</li> </ul> </li> <li>• 40-QFN-0505               <ul style="list-style-type: none"> <li>- I/O pins: 29</li> </ul> </li> <li>• 32-QFN-0505               <ul style="list-style-type: none"> <li>- I/O pins: 22</li> </ul> </li> <li>• Each pin can be set for one of the following modes:               <ul style="list-style-type: none"> <li>- Push-pull output</li> <li>- Open drain output</li> <li>- Input</li> </ul> </li> <li>• The use of each pin can be set by setting the register</li> <li>• Corresponding pin can be configured as an external interrupt source, either the level-trigger/edge-trigger interrupt or the rising-edge/ falling-edge/ both-edge interrupt</li> <li>• Pull-up or pull-down resistor, and debouncing can be set for each pin</li> <li>• Each pin bit can be individually set/reset</li> <li>• Wake-up events triggered by external asynchronous inputs</li> </ul>
Direct Memory Access (DMA) Controller	<ul style="list-style-type: none"> <li>• 4-channel Direct Memory Access (DMA) supporting peripherals</li> <li>• 8-bit/16-bit/32-bit data transfers</li> <li>• Compatible with 19 different types of peripherals</li> <li>• SPI0, SPI1, USART10, USART11, USART12, USART13, I2C0, I2C1, I2C2, ADC</li> </ul>

**Table 3. A31G336 Features (continued)**

Item		Description
General Purpose Timer	16-bit Timer	<ul style="list-style-type: none"> <li>• General-purpose 16-bit up-count timer</li> <li>• 6 channels <ul style="list-style-type: none"> <li>- Timer 1n capture port (T1nCAP) input channels</li> <li>- Timer 1n output port (T1nOUT) output channels</li> </ul> </li> <li>• Timer operating modes <ul style="list-style-type: none"> <li>- Timer/counter mode</li> <li>- Capture mode</li> <li>- PPG one-shot mode</li> <li>- PPG repeat mode</li> </ul> </li> <li>• Interrupt events <ul style="list-style-type: none"> <li>- Timer/counter match interrupt</li> <li>- Timer capture interrupt</li> </ul> </li> <li>• Input clock selection <ul style="list-style-type: none"> <li>- PCLK clock divided by prescaler is selectable</li> <li>- External clock is selectable</li> </ul> </li> <li>• Timer signals can be generated through T1nOUT pins</li> <li>• 12-bit prescaler</li> </ul>
	32-bit Timer	<ul style="list-style-type: none"> <li>• General-purpose 32-bit up-count timer</li> <li>• 2 channels <ul style="list-style-type: none"> <li>- Timer 2n capture port (T2nCAP) input channels</li> <li>- Timer 2n output port (T2nOUT) output channels</li> </ul> </li> <li>• Timer operating modes <ul style="list-style-type: none"> <li>- Timer/counter mode</li> <li>- Capture mode</li> <li>- PPG one-shot mode</li> <li>- PPG repeat mode</li> </ul> </li> <li>• Interrupt events <ul style="list-style-type: none"> <li>- Timer/counter match interrupt</li> <li>- Timer capture interrupt</li> </ul> </li> <li>• Input clock selection <ul style="list-style-type: none"> <li>- PCLK clock divided by prescaler is selectable</li> <li>- External clock is selectable (T20, T21)</li> <li>- LSE clock is selectable (T20)</li> </ul> </li> <li>• Timer signals can be generated through T2nOUT pins</li> <li>• 12-bit prescaler</li> </ul>
System Timer	WDT	<ul style="list-style-type: none"> <li>• 24-bit down-count timer</li> <li>• Reset generation</li> <li>• Window match interrupt</li> <li>• Underflow interrupt</li> <li>• LSI or PCLK is selectable</li> </ul>
	RTCC	<ul style="list-style-type: none"> <li>• Calendar with 0.5 seconds, seconds, minutes, hours, day, week, month, and year up to 2099</li> <li>• Time error correction function</li> <li>• Alarm function with interrupt</li> <li>• Wake-up possible from DEEP SLEEP mode</li> </ul>

**Table 3. A31G336 Features (continued)**

Item	Description	
Communication Interface	USART	<ul style="list-style-type: none"> <li>• 4 channels for asynchronous, synchronous, and serial peripheral interfaces</li> <li>• Asynchronous/synchronous modes (UART)</li> <li>• 5- to 9-bit data transfers</li> <li>• Even/Odd/Non-parity generation and checking</li> <li>• 1-bit or 2-bit stop bit generation and checking</li> <li>• 12-bit baud rate generator</li> <li>• Receive time out function from start bit (Asynchronous only)</li> <li>• Receive character detection</li> <li>• Auto baud rate detection</li> <li>• 1-wire half-duplex communication</li> <li>• Local interconnection network (LIN)</li> <li>• Tx break transmit and Rx break detection</li> <li>• Serial peripheral interface (SPI)</li> <li>• Master/slave operation</li> <li>• Loop-back function</li> <li>• 8-bit data transmit/receive</li> <li>• Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available</li> </ul>
	SPI	<ul style="list-style-type: none"> <li>• Two synchronous serial communication port channels</li> <li>• Master/slave operation</li> <li>• Loop-back mode</li> <li>• Programmable and flexible communication               <ul style="list-style-type: none"> <li>- 8-bit data transmit/receive</li> <li>- SPI clock speed</li> <li>- Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available</li> </ul> </li> </ul>
	I2C	<ul style="list-style-type: none"> <li>• Standard I2C communication protocol</li> <li>• Three channels supported</li> <li>• Master and slave modes supported for each channel</li> <li>• 7-bit addressing supported for slave mode</li> <li>• SCL signal's high/low periods and SDA signal's hold time settable</li> </ul>
	USB	<ul style="list-style-type: none"> <li>• USB 2.0 Full-Speed devices</li> <li>• Crystal-less with clock management unit (HSICMU)</li> <li>• 1024 bytes packet buffer memory SRAM</li> <li>• Number of endpoints from 1 to 5 in addition to Endpoint 0</li> <li>• IN and OUT Endpoint</li> <li>• USB DMA 2 channels, 64 bytes buffer size.</li> </ul>
High Speed Internal OSC Clock Management Unit (HSICMU)	<ul style="list-style-type: none"> <li>• Selectable synchronization signal source               <ul style="list-style-type: none"> <li>- USB SOF (Start of Frame) sent received toggle</li> <li>- LSE</li> <li>- External pin (PD5)</li> </ul> </li> </ul>	
12-bit A/D Converter	ADC	<ul style="list-style-type: none"> <li>• 16 analog input channels</li> <li>• Software and timer match signal triggers supported</li> <li>• Conversion modes and over sampling supported</li> </ul>

**Table 3. A31G336 Features (continued)**

Item		Description
Comparator	CMP	<ul style="list-style-type: none"> <li>• External analog inputs</li> <li>• Hysteresis function</li> <li>• Low and fast speed selectable</li> <li>• Wake-up possible from DEEP SLEEP mode</li> </ul>
Cyclic Redundancy Check	CRC	<ul style="list-style-type: none"> <li>• CRC operating modes:               <ul style="list-style-type: none"> <li>- CRC-CCITT (0x1021)</li> <li>- CRC-16 (0x8005)</li> </ul> </li> <li>• Auto and user mode supported</li> </ul>
Temperature Sensor	TS	<ul style="list-style-type: none"> <li>• -40°C to +85°C wide range of operating temperature</li> <li>• A down counter at 20-bit intervals to count the frequency of the TS</li> <li>• A 24-bit data register to store the count value of the temperature sensor frequency</li> </ul>
Operating Voltage		1.8 V to 5.5 V
Operating Temperature	Commercial Grade	-40°C to 85°C
Package		<ul style="list-style-type: none"> <li>• Six types of package options               <ul style="list-style-type: none"> <li>- 64-LQFP-1010 (0.5 mm pitch)</li> <li>- 64-LQFP-1212 (0.65 mm pitch)</li> <li>- 48-LQFP-0707 (0.5 mm pitch)</li> <li>- 48-QFN-0505 (0.35 mm pitch)</li> <li>- 40-QFN-0505 (0.40 mm pitch)</li> <li>- 32-QFN-0505 (0.50 mm pitch)</li> </ul> </li> </ul>

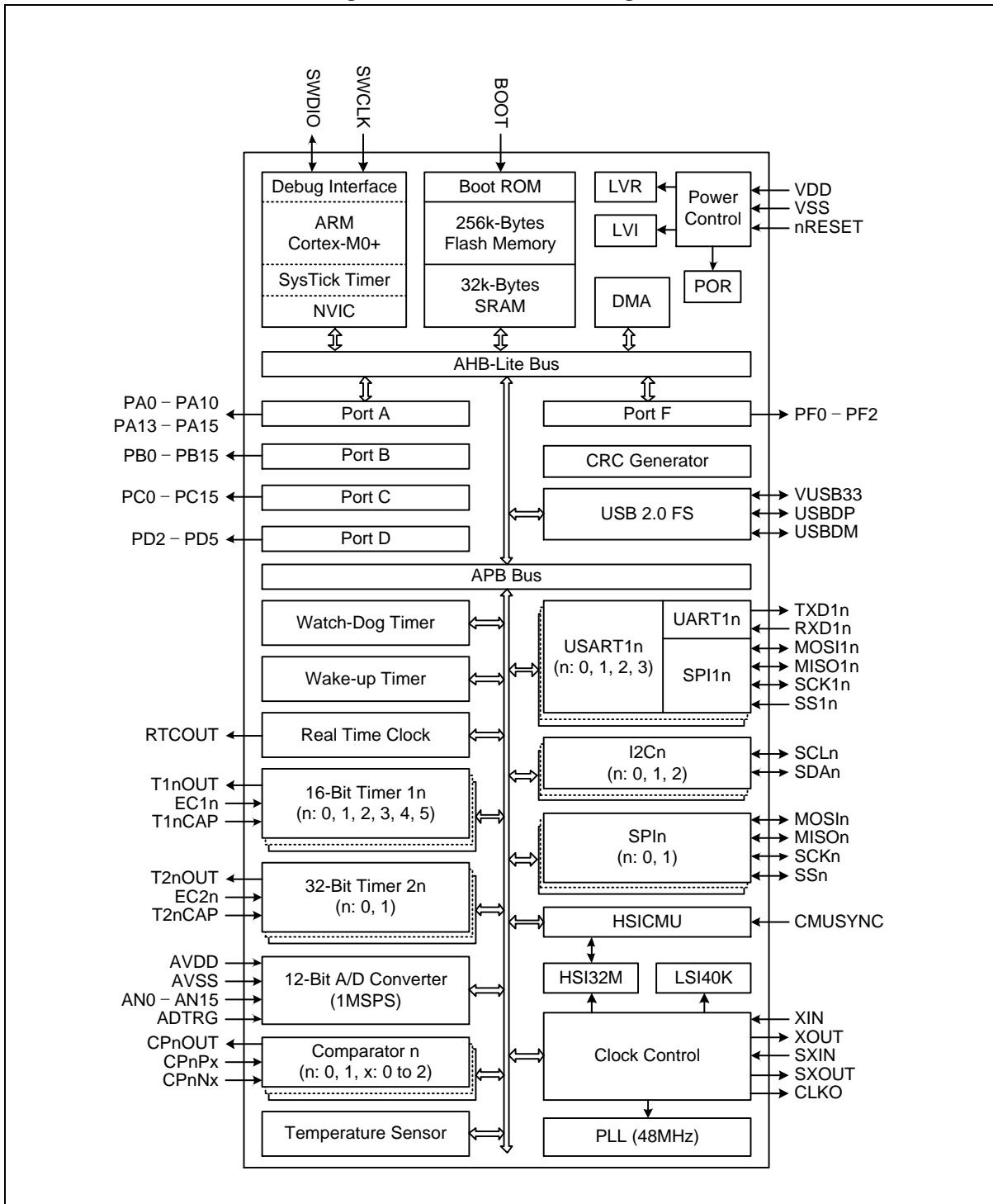
**Table 4. Summary of A31G336 Peripherals**

Peripheral		A31G336RL A31G336RM	A31G336CL	A31G336CU	A31G336IU	A31G336KU
Code Flash Memory		256 KB	256 KB	256 KB	256 KB	256 KB
SRAM		32 KB	32 KB	32 KB	32 KB	32 KB
Timers	General Purpose	8	8	8	8	8
	SysTick	1	1	1	1	1
	Watchdog	1	1	1	1	1
	RTCC	1	1	1	1	1
Communication Interfaces	USB	1	1	1	1	1
	USART	4	4	4	3	2
	I2C	3	3	3	3	3
	SPI	2	2	2	1	1
Direct Memory Access (DMA)		4	4	4	4	4
GPIO		53	37	37	29	22
ADC Number of channels		1 Msps	1 Msps	1 Msps	1 Msps	1 Msps
		16	10	10	9	8
Max. Operating Frequency		48 MHz	48 MHz	48 MHz	48 MHz	48 MHz
CRC		1	1	1	1	1
Operating Voltage		1.8 V to 5.5 V				
Operating Temperature	Commercial	-40°C to 85°C				
Package		64-LQFP-1010 64-LQFP-1212	48LQFP-0707	48QFN-0505	40QFN-0505	32QFN-0505

### 2.3 Block Diagram

Figure 1 shows a block diagram of the A31G336.

**Figure 1. A31G336 Block Diagram**



## 2.4 Functional Overview

The following sections provide overviews of the features of the A31G336 microcontroller.

### 2.4.1 Cortex-M0+ Core

The A31G336 microcontroller uses the energy efficient Cortex-M0+ core from Arm, which is optimized for low-power consumption and features highly efficient 32-bit architecture. The Cortex-M0+ is based on the ARMv6-M Thumb instruction set and includes 16-bit instructions with Thumb-2 technology, allowing for improved performance and energy efficiency. It also includes a simple 24-bit system timer (SYSTICK) that can function as a real-time operating system or a counter. Additionally, the Cortex-M0+ features an integrated Nested Vectored Interrupt Controller (NVIC) for deterministic interrupt handling, hardware single-cycle multiplication for efficient computation, and supports SWD debugging features.

Refer to the technical reference manual **ARM DDI 0484C** for detailed information on Cortex-M0+.

### 2.4.2 On-Chip SRAM

The A31G336 has a block of 0-wait on-chip SRAM. The size of the SRAM is 32 KB, and its base address is 0x2000\_0000. The SRAM memory area is commonly utilized for storing data and as a stack memory. Additionally, it can also be utilized for storing program code for faster execution or during Flash erasing/programming operations.

### 2.4.3 Boot Configuration

The A31G336 has a boot mode option to program internal Flash memory. Boot mode can be entered by setting BOOT pin to 'L' at reset timing (Normal state is 'H').

Boot mode supports the UART boot which uses the UART interface to transmit and receive boot data (TXD10/RXD10).

The pins for the boot mode are listed in Table 5.

**Table 5. Boot Mode Pin List**

Block	Pin Name	Pin Direction	Description
SYSTEM	nRESET	Input	Reset Input signal.
	BOOT/PD5	Input	Set the boot mode.
UART mode of USART10	RXD10/PA3	Input	Receive the UART boot data.
	TXD10/PA2	Output	Transmit the UART boot data.

#### 2.4.4 Operating Voltage

The device operates with a supply voltage of a 1.8 V to 5.5 V (VDD).

During a power-up process, a reset plays an important role and affects the entire process of the system booting. The A31G336 has two power-related reset options as described below:

- POR\_RST (Power-On Reset): Controls the voltage less than 1.4 V
- LVR\_RST (Low-Voltage Reset): Controls the voltage less than 1.68 V (configuration option)

If the power level is higher than the POR and lower than the Flash operating voltage (min. 1.35 V), the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVR\_RST generates the nSYSRESET internal signal, and the microcontroller enters the reset mode to prevent the abnormal operation. To ensure stable operation, it is recommended to select a voltage level higher than the minimum level of 1.68 V that can be set by the LVR.

## 2.4.5 Operation Mode

### 2.4.5.1 Transition of Operation Mode

The INIT mode is the initial state of the chip when a reset is asserted. In RUN mode, the CPU operates at the maximum performance with the high-speed clock system. The SLEEP and DEEP-SLEEP modes are available as low-power consumption modes. During these modes, the processor core and any unused peripherals are halted to effectively manage power consumption.

### 2.4.5.2 RUN Mode

In RUN mode, the CPU and peripheral hardware operate with a high-speed clock. After a reset, the system will enter the RUN mode if the INIT state is detected.

### 2.4.5.3 SLEEP Mode

When the microcontroller enters the SLEEP mode, the CPU is halted while peripheral functions remain active. Users can determine which peripherals are active or inactive in the SLEEP mode by setting the corresponding function enable bit and clock enable bit in the SCU\_PPCLKEN register.

### 2.4.5.4 DEEP-SLEEP Mode

In the DEEP-SLEEP mode, both the CPU and a selected system clock (MCLK) are halted to reduce power consumption. However, the Real time clock/calendar with a sub-clock and the watchdog timer with LSI can still operate in this mode.

### 2.4.5.5 Reset Mode

The A31G336 has two system reset types: a cold reset, which is effective during power up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of the A31G336 are as follows:

- nRESET pin
- Watchdog Timer (WDT) reset
- Low-Voltage Reset (LVR)
- Monitor (MON) reset
- Software reset
- CPU request reset

## 2.4.6 Clocks and Startup

The A31G336 has two main operating clocks: HCLK, which generates clock signals for the CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

### 2.4.6.1 HCLK Clock

The Cortex-M0+ core requires two clocks: HCLK and FCLK. While the HCLK supplies the clock for both the CPU and AHB, the FCLK remains enabled unless the system enters the DEEP-SLEEP mode. Conversely, during the SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 48 MHz, the HCLK frequency must not exceed 48 MHz.

### 2.4.6.2 PCLK Clock

The PCLK can be used as a clock source for any peripherals. The SCU\_PPCLKEN registers determine whether the PCLK is enabled or disabled for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in the DEEP-SLEEP mode.

### 2.4.6.3 Clock Configuration Procedure

Initially, after power on, the HSI (2 MHz) is enabled as a system clock source by default in the system operation sequence. The HSI operates as a system clock until users configure other clock sources according to their needs.

To enable the HSE and LSE clocks, users can set the HSEEN and LSEEN bits in the SCU\_CLKSRCR register. However, before enabling the HSE and LSE blocks, users must first configure the pin mux settings for the XIN/XOUT and SXIN/SXOUT functions. Note that PF0/PF1 and PC14/PC15 pins are shared between these functions, and thus the PF\_MOD/PC\_MOD and PF\_AFSR1/PC\_AFSR2 registers must be configured correctly.

Once the HSE and LSE clocks are enabled, users can verify the stability of the crystal oscillation by using the clock monitoring control register, SCU\_CMONCR. However, it is important to wait at least 10 ms to ensure that the crystal oscillation is stable before changing the system clock.

### 2.4.7 Nested Vectored Interrupt Controller (NVIC)

The A31G336 incorporates the Nested Vector Interrupt Controller (NVIC), which can manage up to 32 maskable interrupt channels with four priority levels. The NVIC in the Cortex-M0+ processor handles and prioritizes interrupts internally within the processor. Software can set the priority of each interrupt, and external interrupt signals are connected to the NVIC, which prioritizes them. The NVIC enables efficient processing of late-arriving interrupts and achieves low-latency interrupt processing. Access to all NVIC registers is only possible through word transfers.

The NVIC has the following advantages:

- Interrupt processing with reduced interrupt latency
- Direct transfer of Interrupt Vector Table (IVT) address to the core
- Fast interrupt processing capability
- Interrupts with higher priority are given precedence over those with lower priority, even if they occur after the lower-priority interrupts.
- Tail Chaining
- Automatic saving of processor state
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

### 2.4.8 Port Control Unit (PCU)

The A31G336 has a Port Control Unit (PCU) module that controls the input and output (I/O) ports. By setting the PCU registers, users can configure the functionality, input/output direction, pull-up/pull-down, and debouncing of the pins for their applications.

### 2.4.9 General-Purpose Input/Output (GPIO)

Pins other than those specified as VDD, GND or certain purpose, can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O pins. Output pins can be configured to output high-level or low-level signals by setting the corresponding bits of the GPIO control register. On the other hand, the input status of logic input pins can be monitored through the control registers.

#### 2.4.10 Embedded Flash Memory

The Flash memory controller serves as an interface between the core and the embedded Flash memory and is responsible for managing the data stored on the Flash memory.

Self-programming is available and ISP and SWD programming is also supported in boot or debugging mode.

The Flash memory of the A31G336 has the following features:

- Code Flash memory for 256 KB with write protection bits
- ECC support
- Erase units
  - Page (512 bytes)
  - Sector (2048 bytes)
  - Bulk (256 KB, full-chip)
- Program unit:
  - Word (4 bytes)
- Code Flash read protection

#### 2.4.11 Direct Memory Access (DMA) Controller

The Direct Memory Access (DMA) controller is used for high-speed data transfers between peripherals and memories. The DMA allows quick data transfers by copying or moving data between memory and peripherals, without involving the core.

- Four channels of direct memory access
- 8-/ 16-/ 32-bit data transfers
- Memory to peripheral transmission
- Peripheral to memory transmission
- DMA transfers are triggered by peripheral interrupts

#### 2.4.12 16-Bit and 32-bit Timers

The A31G336 includes six 16-bit and two 32-bit Timers that offer four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can select an input clock source for the 16-bit and 32-bit Timers, either a divided PCLK or an external clock. Especially for the 32-bit timer 20, LSE can be selected as an input clock source. An internal 12-bit prescaler allows to generate a variety of base clocks for the timers.

When the timer operates in Periodic Mode, interrupts can be triggered at regular intervals. In PWM Mode, users can set the period and duty to generate a PWM signal. In One-shot mode, the timer can generate one PWM waveform. In Capture Mode, the timer can measure pulse intervals of an external input signal based on the predefined conditions. In addition, the timer can transmit signals to control other devices and is primarily used as a periodic tick timer or as a wake-up source.

#### 2.4.13 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is used to detect errors in the microcontroller caused by external interference or unexpected logical conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A31G336 is a 24-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches 0.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

#### 2.4.14 Real Time Clock and Calendar (RTCC)

A real time clock and a calendar can run in SLEEP and DEEP SLEEP modes. The RTCC is not reset by a system reset except in the event of a power-on reset. The internal structure of the RTCC is implemented with the clock source select circuit, second/minute/hour/week/month/year counter circuits, alarm circuit, output select circuit, and error correction circuit.

The RTCC is an independent BCD counter. The main operations of the RTCC include the following:

- Calendar counting 0.5 seconds, seconds, minutes, hours, days, weeks, months, and years up to 2099
- Time error correction function
- Alarm function with interrupt
- Wake-up possibility from DEEP SLEEP mode

#### 2.4.15 Universal Synchronous and Asynchronous Receiver Transmitter (USART)

The A31G336 has a four-channel USART module. The USART module supports UART and SPI modes and features as follows:

- Full duplex operation with independent serial receive and transmit registers
- Asynchronous or synchronous communication
- Baud rate generator
- Supports serial frames with 5- to 9-bit data transfer length and 1 or 2 stop bits generation and checking
- Even/Odd/Non-parity generation and checking-
- Receive character detection and receive time-out function
- Local Interconnection Network (LIN)
- Data over-run detection
- Framing error detection
- Supports three types of interrupts: TX completion, TX data register empty and RX completion
- Double speed asynchronous communication mode
- Up to 8 MHz data transfer in SPI mode

#### 2.4.16 Serial Peripheral Interface (SPI)

The A31G336 has two built-in Serial Peripheral Interface (SPI) modules, which are clock-synchronized, and allow for customizable transmission clock specifications.

The SPI modules facilitate communications between one master and multiple slaves, which can be chosen using the Slave Select (SS) signal. Using four signal terminals (SS, SCK, MOSI, and MISO), the SPI module enables three or four-wire synchronous transfers. Its Transmit and Receive Buffers are separate, which enables full-duplex communication and simultaneous reading and writing of data.

### 2.4.17 Inter-Integrated Circuit (I2C) Interface

The Inter-Integrated Circuit (I2C) interface built in the A31G336 is compliant with the standard I2C communication protocol. It is used for serial communication between internal and external devices via the I2C protocol.

The built-in I2C interface, equipped with three units, supports both master and slave modes and is capable of transmitting and receiving data in bytes by using interrupts or polling.

The I2C of the A31G336 operates in Standard mode (100 kHz), Fast mode (400 kHz) or Fast Plus mode (1 MHz). In addition, it also supports General call.

The I2C interface facilitates communication with multiple peripherals that share the same bus type. To utilize I2C, it is recommended to configure the SCL and SDA pins as open-drain and attach external pull-up resistors to ensure that their output signals are maintained in a high-level.

**Table 6. Features of I2Cn (n = 0 to 2)**

I2C Features	I2C0	I2C1	I2C2
7-bit addressing mode	○	○	○
Standard mode (up to 100 kbit/s)	○	○	○
Fast mode (up to 400 kbit/s)	○	○	○
Fast Plus mode (up to 1,000 kbit/s)	○	○	○
General call	○	○	○

### 2.4.18 Analog-to-Digital Converter (ADC)

The A31G336 is equipped with a 12-bit Analog-to-Digital Converter (ADC) module that supports up to 16 analog inputs. It can convert analog signals to digital signals at a conversion rate of up to 1 Msps. 19-channel analog MUX provides various combinations of data from external and internal analog signals. The A/D module supports single, sequential, and continuous conversion modes.

#### 2.4.19 Cyclic Redundancy Check (CRC) Calculation Module

The A31G336 has a built-in Cyclic Redundancy Check (CRC) module capable of computing 16-bit CRC codes from data streams and Flash memories. CRC-based techniques are commonly used to ensure the integrity of data transmission or storage and can also be used to verify the integrity of Flash memory in compliance with functional safety standards. By computing a signature of the software during runtime and comparing it with a reference signature, the CRC module can help detect any changes made to the software.

The CRC module in the A31G336 offers the following features:

- Auto CRC and user CRC mode
- Supports CRC-CCITT ( $G1(x) = x^{16} + x^{12} + x^5 + 1$ )
- Supports CRC-16 ( $G2(x) = x^{16} + x^{15} + x^2 + 1$ )
- CRC and checksum mode
- CRC/checksum start address auto increment (user mode only)

#### 2.4.20 Comparator

The A31G336 has two comparator blocks. The block has an internal reference for channels. There are four modes for each comparator: ultra-low power mode, low power mode, medium power mode, and high-speed mode. A comparator can run in SLEEP and DEEP SLEEP modes.

#### 2.4.21 Temperature Sensor (TS)

The temperature sensor consists of a ring-oscillator. Its frequency varies with temperature. It can be used to measure the junction temperature of the device.

#### 2.4.22 Universal Serial Bus (USB)

The USB block of A31G336 series controls USB 2.0 full speed interface. The USB block features the following:

- Support for Full-Speed (FS, 12-Mbps)
- Configurable number of endpoints from 1 to 5
  - IN and OUT Endpoint
- USB DMA 2-channels, 64 bytes buffer size

## 2.5 Development Tools

In this chapter, various development tools for the A31G336 are described. ABOV provides software tools, debuggers, and programmers to assist users in achieving the desired results for their target applications. ABOV supports the complete development ecosystem for our customers.

### 2.5.1 Compiler

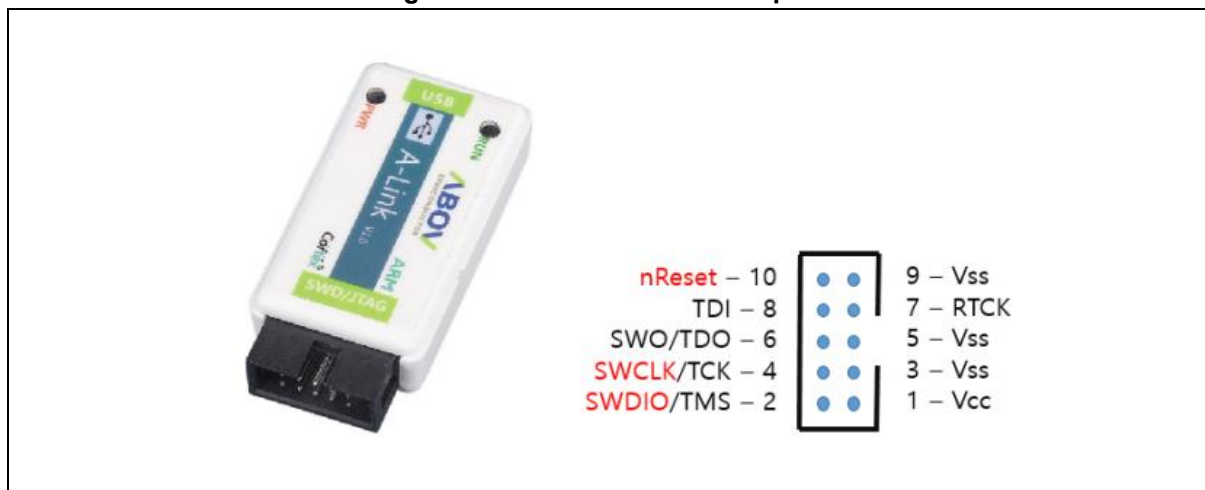
Since the A31G336 has the ARM 32-bit Cortex-M0+ core, any third-party compiler, such as Keil, IAR and GCC cross-C compiler supporting Cortex-M0+, is available.

### 2.5.2 Debugger

A-Link and A-Link Pro can be used to emulate the A31G336 microcontroller using the SWD interface and have a two-wire interface to connect to the microcontroller on the user system. A-Link and A-Link Pro provide extensive debugging capabilities for the microcontroller, including the ability to read or write the value of the microcontroller's internal memory and I/O peripherals, as well as control its internal debugging logic. A-Link and A-Link Pro are debug interfaces with third-party compilers, providing an excellent combination of debugging environments.

The figure below shows the pinout for programming with the A-Link and A-Link Pro. For more detailed information about the A-Link and A-Link Pro, please visit [www.abovsemi.com](http://www.abovsemi.com) and download related software and documents.

**Figure 2. A-Link and Pin Description**



### 2.5.3 Programmer

#### 2.5.3.1 E-PGM+ and E-PGM Serial

E-PGM+ and E-PGM Serial are standalone programmers, which allow users to program directly on the device.

- Supports for all ABOV microcontrollers
- Dedicated tool for mass production
- 40-pin Textool DIP socket for single chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls

#### 2.5.3.2 Gang Programmer

E-Gang4 and E-Gang6 can program multiple devices simultaneously and operate in host-controlled and standalone modes without requiring a host computer connection. These programmers feature a USB interface for easy connection to a handler.

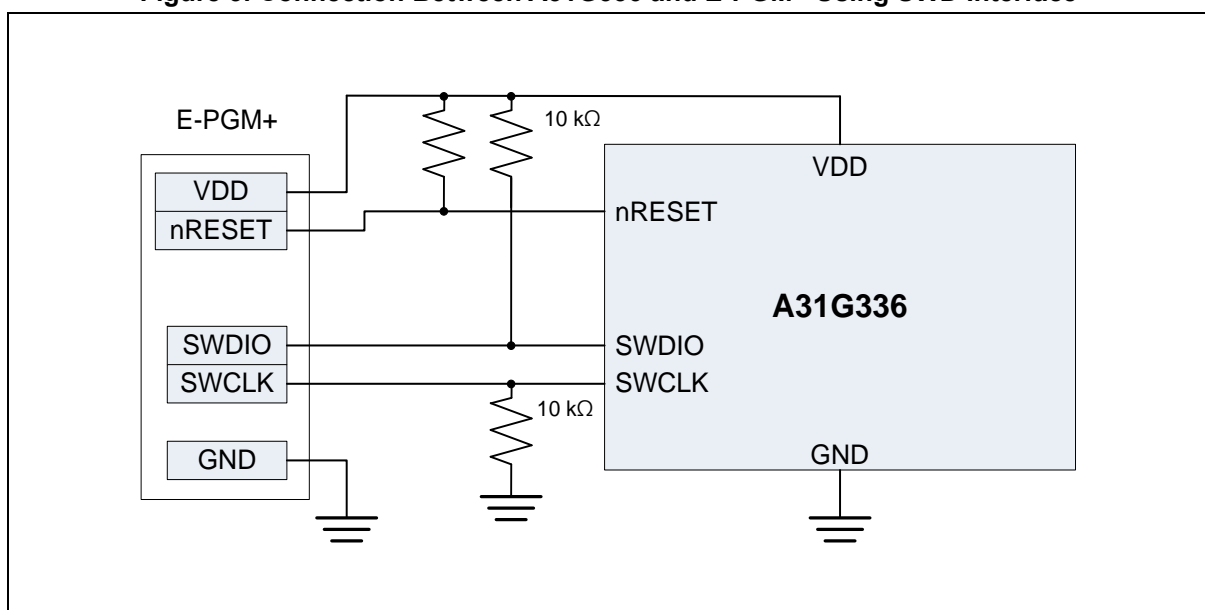
**NOTE:**

1. Visit the [ABOV homepage](#) and refer to the "Tools & Support > Programmer" menu.

#### 2.5.3.3 SWD Mode and E-PGM+ Connections

The connection between the A31G336 and E-PGM+ using the SWD interface is illustrated in Figure 3.

**Figure 3. Connection Between A31G336 and E-PGM+ Using SWD Interface**



### 3. Pinouts and Pin Descriptions

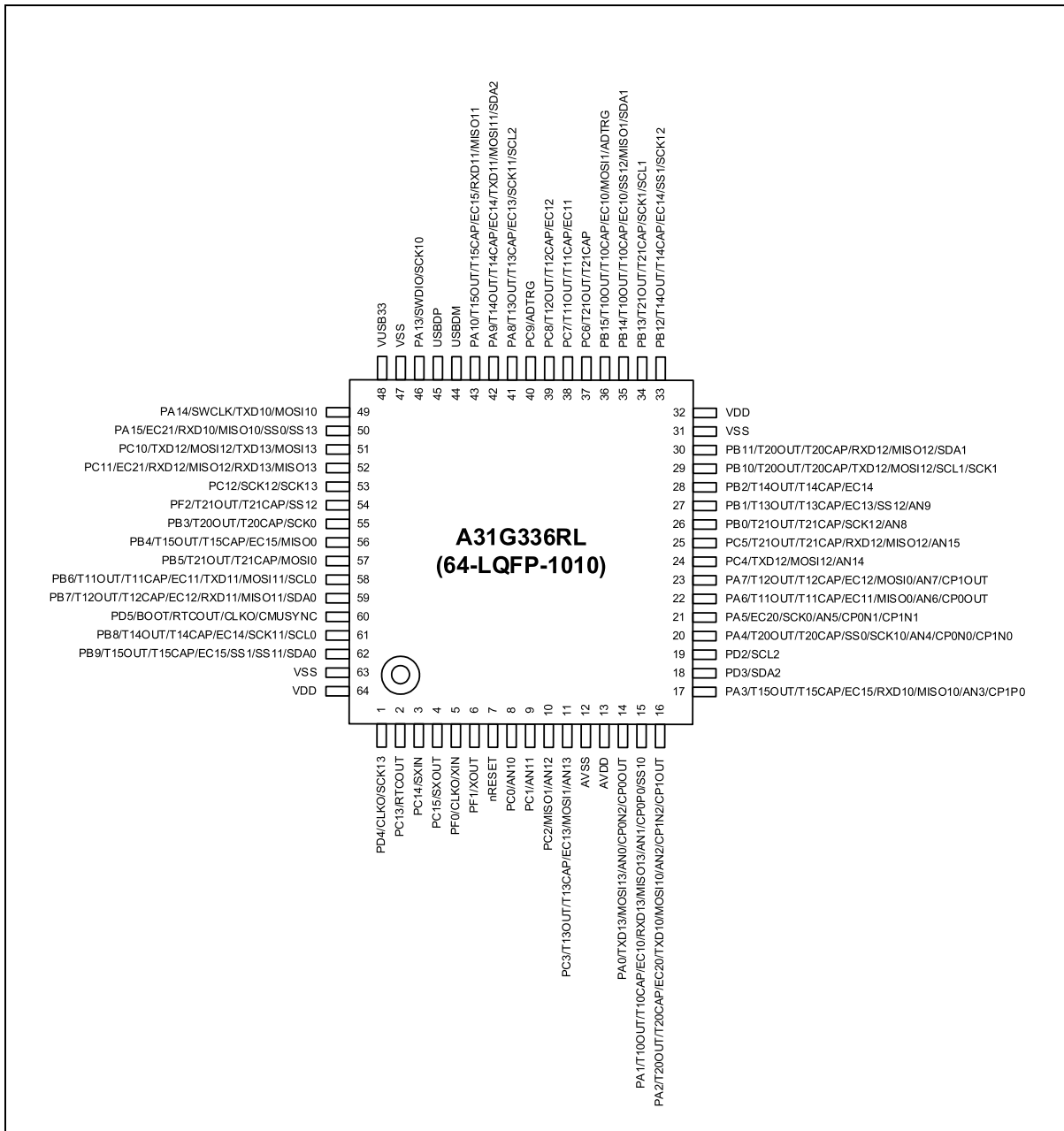
In this chapter, pinouts and pin descriptions of the A31G336 are described.

#### 3.1 Pinouts

Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, and Figure 9 show the top view of the packages.

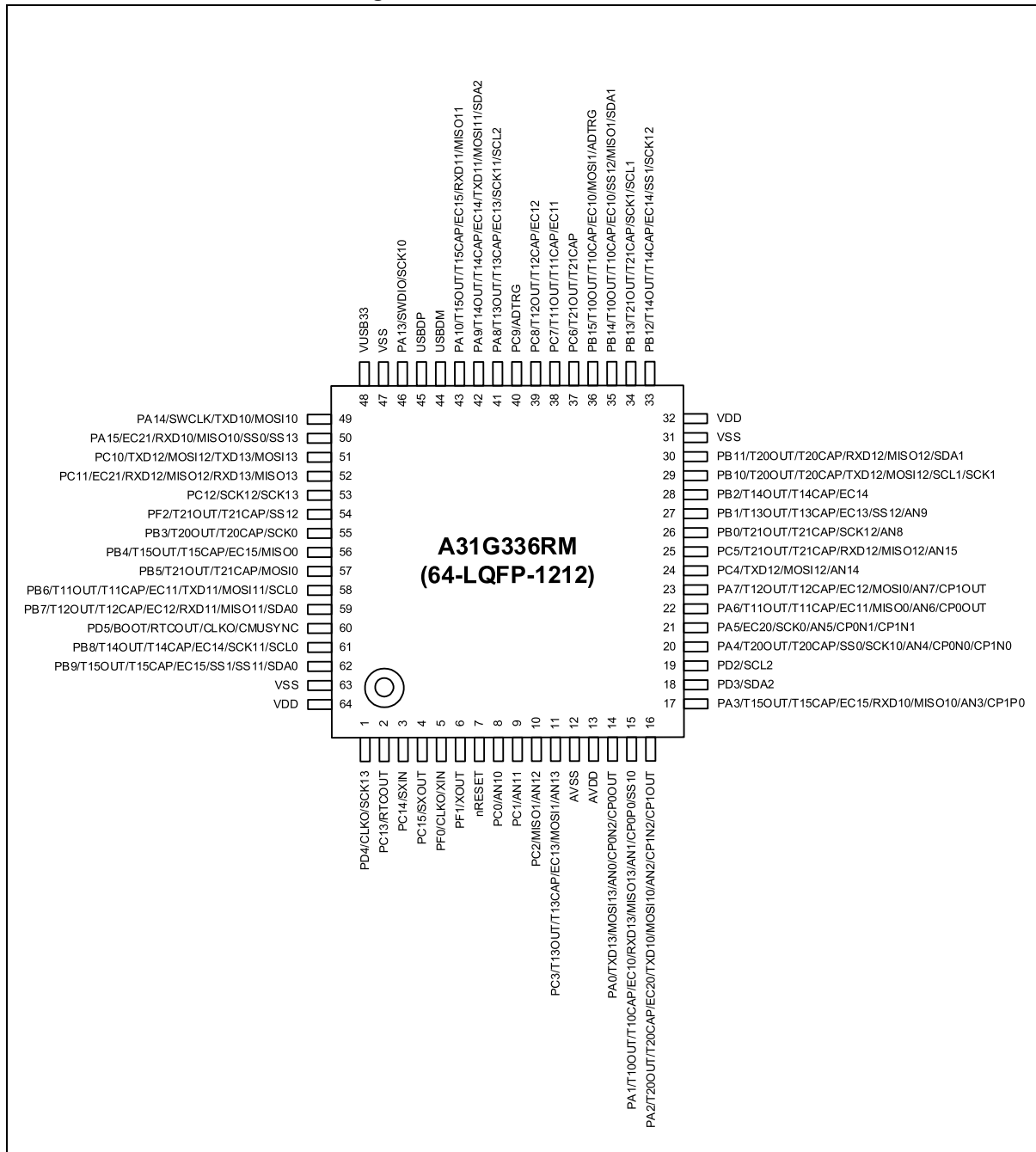
##### 3.1.1 A31G336RL (64-LQFP-1010)

Figure 4. 64-LQFP-1010 Pinouts



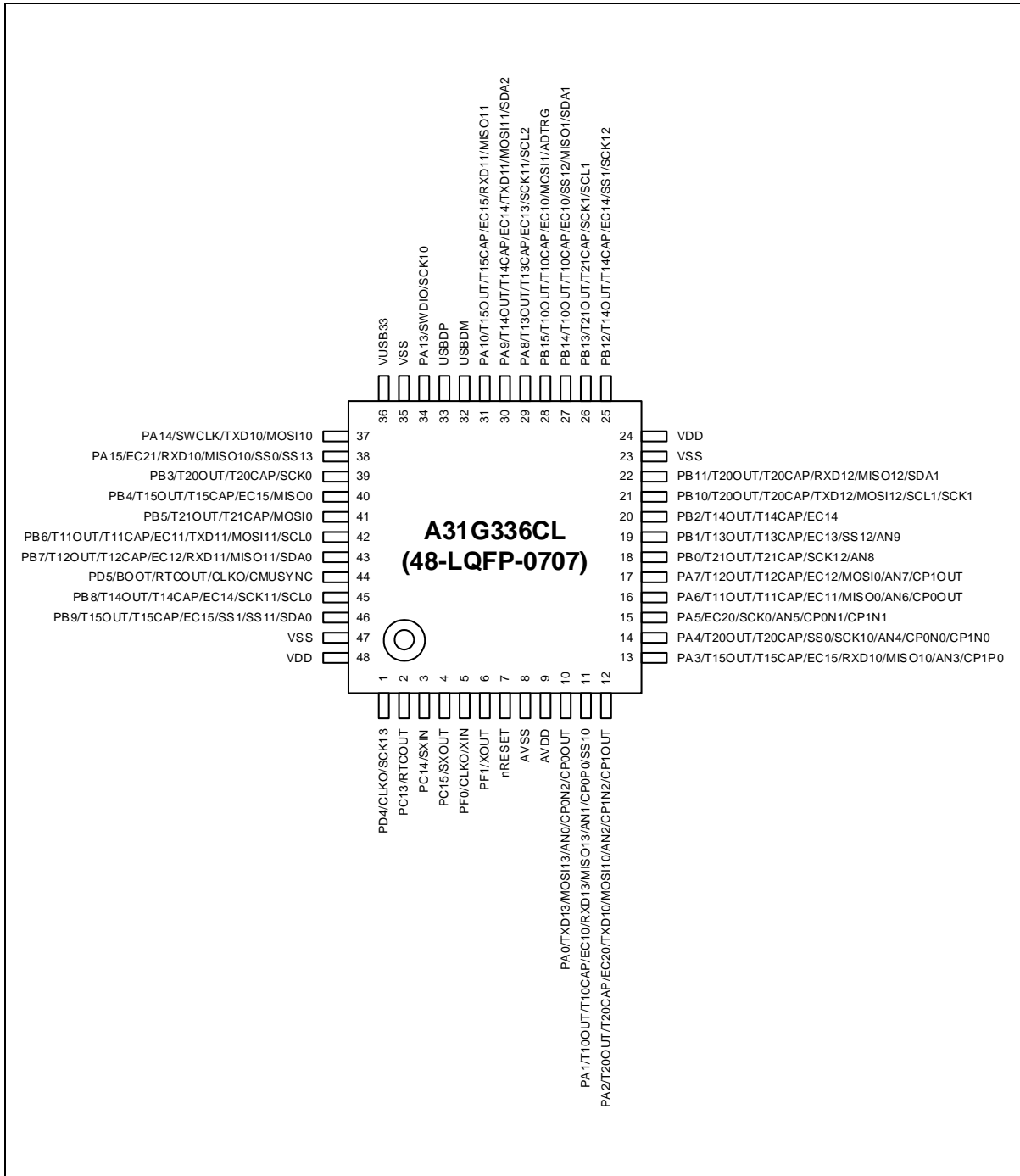
3.1.2 A31G336RM (64-LQFP-1212)

Figure 5. 64-LQFP-1212 Pinouts



3.1.3 A31G336CL (48-LQFP-0707)

Figure 6. 48-LQFP-0707 Pinouts

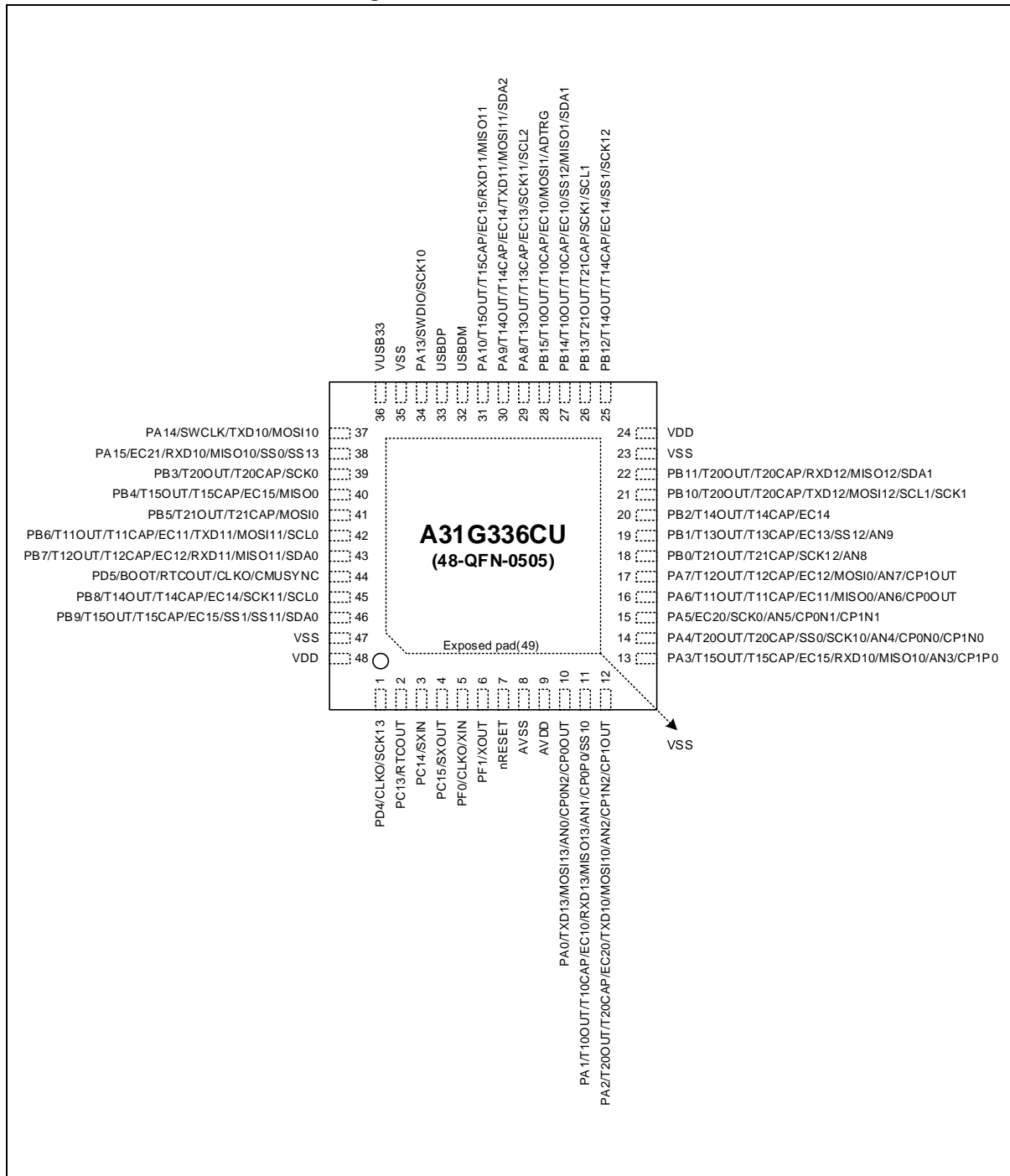


NOTE:

- When using the 48-LQFP package, each of the PC[12:0], PD[3:2], and PF[2] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.4 A31G336CU (48-QFN-0505)

Figure 7. 48-QFN-0505 Pinouts

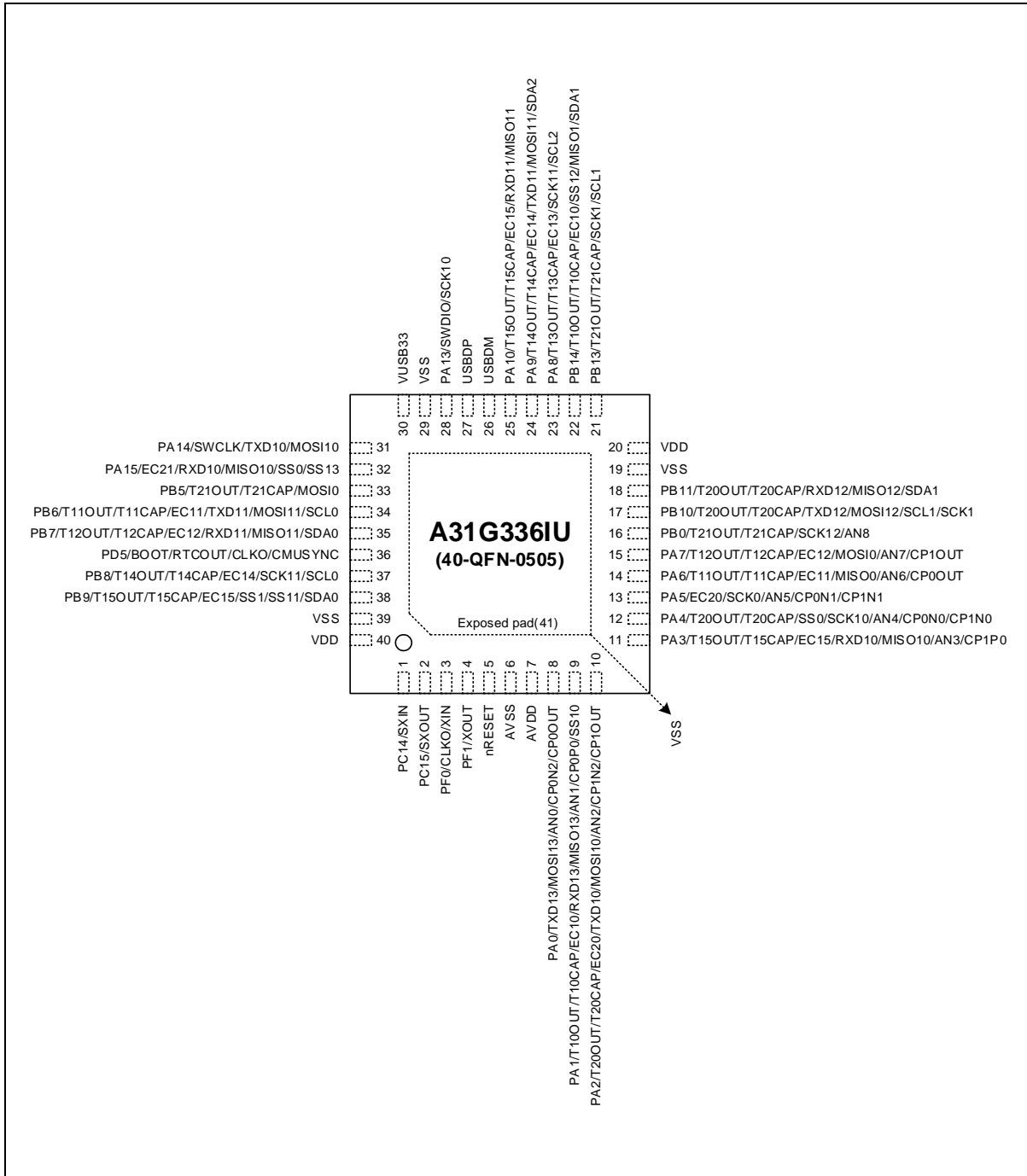


NOTE:

- When using the 48-QFN package, each of the PC[12:0], PD[3:2], and PF[2] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.5 A31G336IU (40-QFN-0505)

Figure 8. 40-QFN-0505 Pinouts

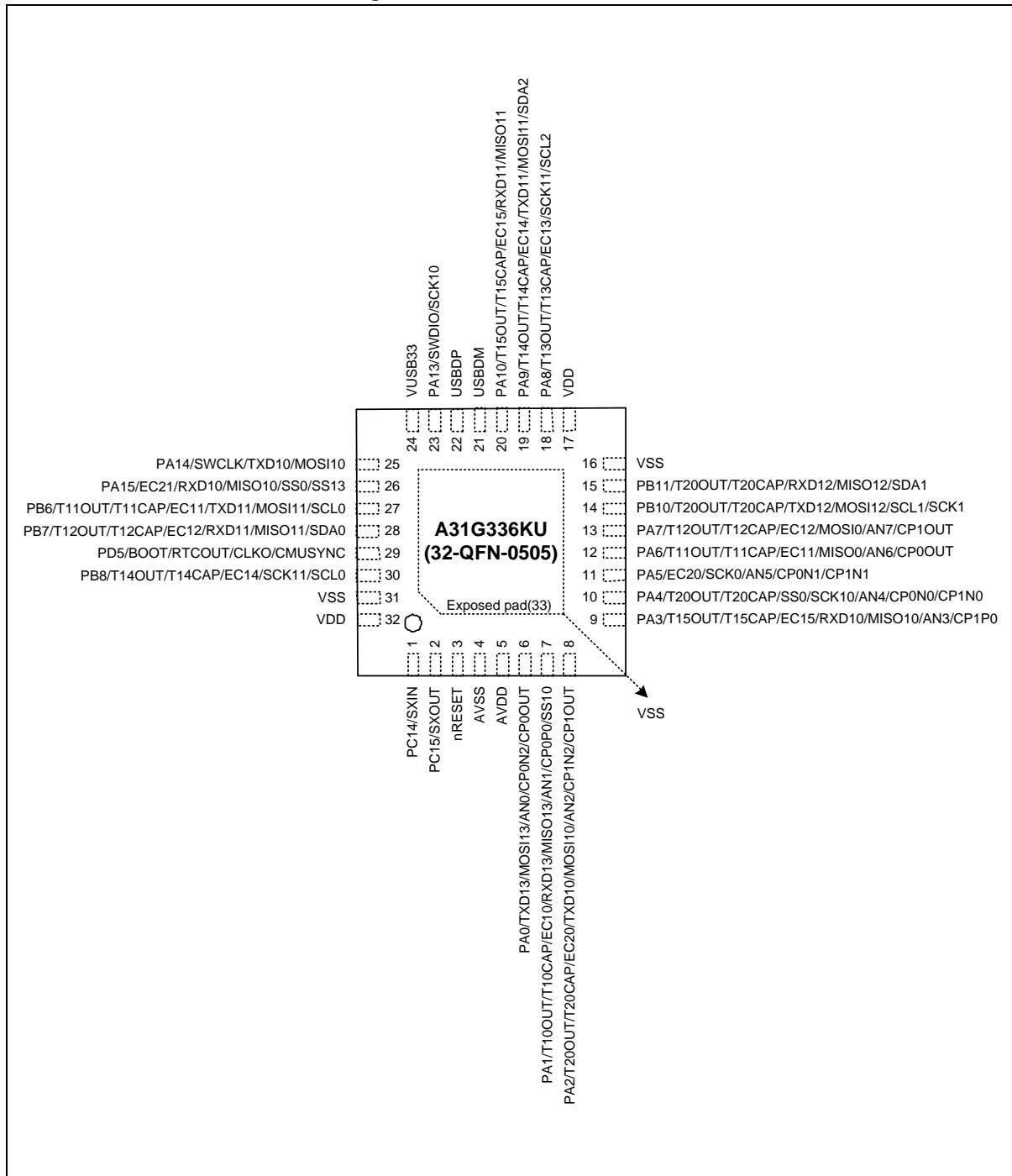


NOTE:

1. When using the 40-QFN package, each of the PB[15, 12, 4:1], PC[13:0], PD[4:2], and PF[2] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.6 76A31G336KU (32-QFN-0505)

Figure 9. 32-QFN-0505 Pinouts



NOTE:

1. When using the 32-QFN package, each of the PB[15:12, 9, 5:0], PC[13:0], PD[4:2], and PF[2:0] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

### 3.2 Pin Description

**Table 7. Legend and Abbreviation Used in Pin Description**

Name	Abbreviation	Definition
Pin name		The pin name remains constant.
Pin type	I	Input
	O	Output
	I/O	Input/Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger input
	C	CMOS input
	A	Analog
	P	Power

Pin configuration information in Table 8 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to eight selections of functions including GPIO.

**Table 8. Pin Description**

Pin Number				Pin Name	Type	Description	Remark
64-Pin	48-Pin	40-Pin	32-Pin				
1	1			PD4 <sup>(1)</sup>	IOUDS	Port D bit 4 input/output	
				CLKO	O	System clock output	
				SCK13	IO	SPI clock input/output	
2	2			PC13 <sup>(1)</sup>	IOUDS	Port C bit 13 input/output	
				RTCOU	O	Real time clock output	
3	3	1	1	PC14 <sup>(1)</sup>	IOUDS	Port C bit 14 input/output	
				SXIN	IA	Sub-oscillator input	
4	4	2	2	PC15 <sup>(1)</sup>	IOUDS	Port C bit 15 input/output	
				SXOUT	OA	Sub-oscillator output	
5	5	3		PF0 <sup>(1)</sup>	IOUDS	Port F bit 0 input/output	
				XIN	IA	Main oscillator input	
				CLKO	O	System clock output	
6	6	4		PF1 <sup>(1)</sup>	IOUDS	Port F bit 1 input/output	
				XOUT	OA	Main oscillator output	
7	7	5	3	nRESET	IU	External reset input	Always pull-up
8				PC0 <sup>(1)</sup>	IOUDS	Port C bit 0 input/output	
				AN10	IA	A/D converter analog input channel	
9				PC1 <sup>(1)</sup>	IOUDS	Port C bit 1 input/output	
				AN11	IA	A/D converter analog input channel	
10				PC2 <sup>(1)</sup>	IOUDS	Port C bit 2 input/output	
				MISO1	IO	SPI master in slave out	
				AN12	IA	A/D converter analog input channel	
11				PC3 <sup>(1)</sup>	IOUDS	Port C bit 3 input/output	
				T13OUT	O	Timer 13 pulse output	
				T13CAP	I	Timer 13 capture input	
				EC13	I	Timer 13 event count input	
				MOSI1	IO	SPI master out slave in	
				AN13	IA	A/D converter analog input channel	
12	8	6	4	AVSS	AP	Analog ground	
13	9	7	5	AVDD	AP	AVDD	
14	10	8	6	PA0 <sup>(1)</sup>	IOUDS	Port A bit 0 input/output	
				TXD13	O	UART data output	
				MOSI13	IO	SPI master out slave in	
				AN0	IA	A/D converter analog input channel	
				CP0N2	IA	Comparator negative input	
				CP0OUT	O	Comparator output	

Table 8. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	40-pin	32-pin				
15	11	9	7	PA1 <sup>(1)</sup>	IOUDS	Port A bit 1 input/output	
				T10OUT	O	Timer 10 pulse output	
				T10CAP	I	Timer 10 capture input	
				EC10	I	Timer 10 event count input	
				RXD13	I	UART data input	
				MISO13	IO	SPI master in slave out	
				AN1	IA	A/D converter analog input channel	
				CP0P0	IA	Comparator positive input	
16	12	10	8	PA2 <sup>(1)</sup>	IOUDS	Port A bit 2 input/output	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				EC20	I	Timer 20 event count input	
				TXD10	O	UART data output	
				MOSI10	IO	SPI master out slave in	
				AN2	IA	A/D converter analog input channel	
				CP1N2	IA	Comparator negative input	
17	13	11	9	PA3 <sup>(1)</sup>	IOUDS	Port A bit 3 input/output	
				T15OUT	O	Timer 15 pulse output	
				T15CAP	I	Timer 15 capture input	
				EC15	I	Timer 15 event count input	
				RXD10	I	UART data input	
				MISO10	IO	SPI master in slave out	
				AN3	IA	A/D converter analog input channel	
				CP1P0	IA	Comparator positive input	
18				PD3 <sup>(1)</sup>	IOUDS	Port D bit 3 input/output	
				SDA2	IO	I2C data input/output	
19				PD2 <sup>(1)</sup>	IOUDS	Port D bit 2 input/output	
				SCL2	IO	I2C clock input/output	
20	14	12	10	PA4 <sup>(1)</sup>	IOUDS	Port A bit 4 input/output	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				SS0	I	SPI slave select input	
				SCK10	IO	SPI clock input/output	
				AN4	IA	A/D converter analog input channel	
				CP0N0	IA	Comparator negative input	
21	15	13	11	PA5 <sup>(1)</sup>	IOUDS	Port A bit 5 input/output	
				EC20	I	Timer 20 event count input	
				SCK0	IO	SPI clock input/output	
				AN5	IA	A/D converter analog input channel	
				CP0N1	IA	Comparator negative input	
				CP1N1	IA	Comparator negative input	

Table 8. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	40-pin	32-pin				
22	16	14	12	PA6 <sup>(1)</sup>	IOUDS	Port A bit 6 input/output	
				T11OUT	O	Timer 11 pulse output	
				T11CAP	I	Timer 11 capture input	
				EC11	I	Timer 11 event count input	
				MISO0	IO	SPI master in slave out	
				AN6	IA	A/D converter analog input channel	
				CP0OUT	O	Comparator output	
23	17	15	13	PA7 <sup>(1)</sup>	IOUDS	Port A bit 7 input/output	
				T12OUT	O	Timer 12 pulse output	
				T12CAP	I	Timer 12 capture input	
				EC12	I	Timer 12 event count input	
				MOSI0	IO	SPI master out slave in	
				AN7	IA	A/D converter analog input channel	
				CP1OUT	O	Comparator output	
24				PC4 <sup>(1)</sup>	IOUDS	Port C bit 4 input/output	
				TXD12	O	UART data output	
				MOSI12	IO	SPI master out slave in	
				AN14	IA	A/D converter analog input channel	
25				PC5 <sup>(1)</sup>	IOUDS	Port C bit 5 input/output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				RXD12	I	UART data input	
				MISO12	IO	SPI master in slave out	
				AN15	IA	A/D converter analog input channel	
26	18	16		PB0 <sup>(1)</sup>	IOUDS	Port B bit 0 input/output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				SCK12	IO	SPI clock input/output	
				AN8	IA	A/D converter analog input channel	
27	19			PB1 <sup>(1)</sup>	IOUDS	Port B bit 1 input/output	
				T13OUT	O	Timer 13 pulse output	
				T13CAP	I	Timer 13 capture input	
				EC13	I	Timer 13 event count input	
				SS12	I	SPI slave select input	
				AN9	IA	A/D converter analog input channel	
28	20			PB2 <sup>(1)</sup>	IOUDS	Port B bit 2 input/output	
				T14OUT	O	Timer 14 pulse output	
				T14CAP	I	Timer 14 capture input	
				EC14	I	Timer 14 event count input	

Table 8. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	40-pin	32-pin				
29	21	17	14	PB10 <sup>(1)</sup>	IOUDS	Port B bit 10 input/output	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				TXD12	O	UART data output	
				MOSI12	IO	SPI master out slave in	
				SCL1	IO	I2C clock input/output	
				SCK1	IO	SPI clock input/output	
30	22	18	15	PB11 <sup>(1)</sup>	IOUDS	Port B bit 11 input/output	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				RXD12	I	UART data input	
				MISO12	IO	SPI master in slave out	
				SDA1	IO	I2C data input/output	
31	23	19	16	VSS	P	Ground	
32	24	20	17	VDD	P	VDD	
33	25			PB12 <sup>(1)</sup>	IOUDS	Port B bit 12 input/output	
				T14OUT	O	Timer 14 pulse output	
				T14CAP	I	Timer 14 capture input	
				EC14	I	Timer 14 event count input	
				SS1	I	SPI slave select input	
				SCK12	IO	SPI clock input/output	
34	26	21		PB13 <sup>(1)</sup>	IOUDS	Port B bit 13 input/output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				SCK1	IO	SPI clock input/output	
				SCL1	IO	I2C clock input/output	
35	27	22		PB14 <sup>(1)</sup>	IOUDS	Port B bit 14 input/output	
				T10OUT	O	Timer 10 pulse output	
				T10CAP	I	Timer 10 capture input	
				EC10	I	Timer 10 event count input	
				SS12	I	SPI slave select input	
				MISO1	IO	SPI master in slave out	
				SDA1	IO	I2C data input/output	
36	28			PB15 <sup>(1)</sup>	IOUDS	Port B bit 15 input/output	
				T10OUT	O	Timer 10 pulse output	
				T10CAP	I	Timer 10 capture input	
				EC10	I	Timer 10 event count input	
				MOSI1	IO	SPI master out slave in	
				ADTRG	I	ADC trigger input	
				37			
T21OUT	O	Timer 21 pulse output					
T21CAP	I	Timer 21 capture input					

Table 8. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	40-pin	32-pin				
38				PC7 <sup>(1)</sup>	IOUDS	Port C bit 7 input/output	
				T11OUT	O	Timer 11 pulse output	
				T11CAP	I	Timer 11 capture input	
				EC11	I	Timer 11 event count input	
39				PC8 <sup>(1)</sup>	IOUDS	Port C bit 8 input/output	
				T12OUT	O	Timer 12 pulse output	
				T12CAP	I	Timer 12 capture input	
				EC12	I	Timer 12 event count input	
40				PC9 <sup>(1)</sup>	IOUDS	Port C bit 9 input/output	
				ADTRG	I	ADC trigger input	
41	29	23	18	PA8 <sup>(1)</sup>	IOUDS	Port A bit 8 input/output	
				T13OUT	O	Timer 13 pulse output	
				T13CAP	I	Timer 13 capture input	
				EC13	I	Timer 13 event count input	
				SCK11	IO	SPI clock input/output	
42	30	24	19	SCL2	IO	I2C clock input/output	
				PA9 <sup>(1)</sup>	IOUDS	Port A bit 9 input/output	
				T14OUT	O	Timer 14 pulse output	
				T14CAP	I	Timer 14 capture input	
				EC14	I	Timer 14 event count input	
				TXD11	O	UART data output	
43	31	25	20	MOSI11	IO	SPI master out slave in	
				SDA2	IO	I2C data input/output	
				PA10 <sup>(1)</sup>	IOUDS	Port A bit 10 input/output	
				T15OUT	O	Timer 15 pulse output	
				T15CAP	I	Timer 15 capture input	
				EC15	I	Timer 15 event count input	
44	32	26	21	RXD11	I	UART data input	
				MISO11	IO	SPI master in slave out	
44	32	26	21	USBDM	IO	USB data line minus. If the USB block is not used, the pin should be connected to a pull-down resistor, either internal or external.	
45	33	27	22	USBDP	IO	USB data line plus. If the USB block is not used, the pin should be connected to a pull-down resistor, either internal or external.	
46	34	28	23	PA13	IOUDS	Port A bit 13 input/output	
				SWDIO <sup>(1)(3)(4)</sup>	I/O	SWD data input/output	Pull-up when reset
				SCK10	IO	SPI clock input/output	
47	35	29		VSS	P	Ground	
48	36	30	24	VUSB33	P	3.3V power input or 3.3 V LDO output for USB block. If the USB block is not used, the VUSB33 pin must be connected to VDD. A 0.1uF capacitor should be connected between this pin and ground.	

Table 8. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	40-pin	32-pin				
49	37	31	25	PA14	IOUDS	Port A bit 14 input/output	
				SWCLK <sup>(1)(3)(4)</sup>	I	SWD clock input	Pull-down when reset
				TXD10	O	UART data output	
				MOSI10	IO	SPI master out slave in	
50	38	32	26	PA15 <sup>(1)</sup>	IOUDS	Port A bit 15 input/output	
				EC21	I	Timer 21 event count input	
				RXD10	I	UART data input	
				MISO10	IO	SPI master in slave out	
				SS0	I	SPI slave select input	
				SS13	I	SPI slave select input	
51				PC10 <sup>(1)</sup>	IOUDS	Port C bit 10 input/output	
				TXD12	O	UART data output	
				MOSI12	IO	SPI master out slave in	
				TXD13	O	UART data output	
				MOSI13	IO	SPI master out slave in	
52				PC11 <sup>(1)</sup>	IOUDS	Port C bit 11 input/output	
				EC21	I	Timer 21 event count input	
				RXD12	I	UART data input	
				MISO12	IO	SPI master in slave out	
				RXD13	I	UART data input	
				MISO13	IO	SPI master in slave out	
53				PC12 <sup>(1)</sup>	IOUDS	Port C bit 12 input/output	
				SCK12	IO	SPI clock input/output	
				SCK13	IO	SPI clock input/output	
54				PF2 <sup>(1)</sup>	IOUDS	Port F bit 2 input/output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				SS12	I	SPI slave select input	
55	39			PB3 <sup>(1)</sup>	IOUDS	Port B bit 3 input/output	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				SCK0	IO	SPI clock input/output	
56	40			PB4 <sup>(1)</sup>	IOUDS	Port B bit 4 input/output	
				T15OUT	O	Timer 15 pulse output	
				T15CAP	I	Timer 15 capture input	
				EC15	I	Timer 15 event count input	
				MISO0	IO	SPI master in slave out	
57	41	33		PB5 <sup>(1)</sup>	IOUDS	Port B bit 5 input/output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				MOSI0	IO	SPI master out slave in	

Table 8. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	40-pin	32-pin				
58	42	34	27	PB6 <sup>(1)</sup>	IOUDS	Port B bit 6 input/output	
				T11OUT	O	Timer 11 pulse output	
				T11CAP	I	Timer 11 capture input	
				EC11	I	Timer 11 event count input	
				TXD11	O	UART data output	
				MOSI11	IO	SPI master out slave in	
				SCL0	IO	I2C clock input/output	
59	43	35	28	PB7 <sup>(1)</sup>	IOUDS	Port B bit 7 input/output	
				T12OUT	O	Timer 12 pulse output	
				T12CAP	I	Timer 12 capture input	
				EC12	I	Timer 12 event count input	
				RXD11	I	UART data input	
				MISO11	IO	SPI master in slave out	
				SDA0	IO	I2C data input/output	
60	44	36	29	PD5	IOUDS	Port D bit 5 input/output	
				BOOT <sup>(1)(5)</sup>	IU	Boot mode input	Pull-up when reset
				RTCOU	O	Real time clock output	
				CLKO	O	System clock output	
				CMUSYNC	I	HSI clock management unit sync input	
61	45	37	30	PB8 <sup>(1)</sup>	IOUDS	Port B bit 8 input/output	
				T14OUT	O	Timer 14 pulse output	
				T14CAP	I	Timer 14 capture input	
				EC14	I	Timer 14 event count input	
				SCK11	IO	SPI clock input/output	
				SCL0	IO	I2C clock input/output	
62	46	38		PB9 <sup>(1)</sup>	IOUDS	Port B bit 9 input/output	
				T15OUT	O	Timer 15 pulse output	
				T15CAP	I	Timer 15 capture input	
				EC15	I	Timer 15 event count input	
				SS1	I	SPI slave select input	
				SS11	I	SPI slave select input	
				SDA0	IO	I2C data input/output	
63	47	39	31	VSS	P	Ground	
64	48	40	32	VDD	P	VDD	

## NOTES:

1. After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the reset value. This configuration is in compliance with the 64-pin standard.
2. Do not configure unused pins as floating inputs.
3. After a reset, the alternate functions of the PA13 and PA14 pins are set as SWDIO and SWCLK, respectively, and the internal pull-down on SWCLK and the internal pull-up on SWDIO are enabled.
4. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.
5. After reset, the PD5 pin is configured as BOOT alternate function and the internal pull-up is activated.

### 3.3 Alternate Function Pins

The GPIO pins have alternate functions as described in Table 9.

**Table 9. GPIO Alternate Functions**

Pin Name	Alternate Function							
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	–	–	TXD13	MOSI13	–	AN0	CP0N2	CP0OUT
PA1	T10OUT	T10CAP	RXD13	MISO13	EC10	AN1	CP0P0	SS10
PA2	T20OUT	T20CAP	TXD10	MOSI10	EC20	AN2	CP1N2	CP1OUT
PA3	T15OUT	T15CAP	RXD10	MISO10	EC15	AN3	CP1P0	–
PA4	T20OUT	T20CAP	SS0	SCK10	–	AN4	CP0N0	CP1N0
PA5	–	–	–	SCK0	EC20	AN5	CP0N1	CP1N1
PA6	T11OUT	T11CAP	–	MISO0	EC11	AN6	–	CP0OUT
PA7	T12OUT	T12CAP	–	MOSI0	EC12	AN7	–	CP1OUT
PA8	T13OUT	T13CAP	–	SCK11	EC13	SCL2	–	–
PA9	T14OUT	T14CAP	TXD11	MOSI11	EC14	SDA2	–	–
PA10	T15OUT	T15CAP	RXD11	MISO11	EC15	–	–	–
PA13	SWDIO	–	–	SCK10	–	–	–	–
PA14	SWCLK	–	TXD10	MOSI10	–	–	–	–
PA15	–	–	RXD10	MISO10	EC21	–	SS0	SS13
PB0	T21OUT	T21CAP	–	SCK12	–	AN8	–	–
PB1	T13OUT	T13CAP	–	SS12	EC13	AN9	–	–
PB2	T14OUT	T14CAP	–	–	EC14	–	–	–
PB3	T20OUT	T20CAP	–	SCK0	–	–	–	–
PB4	T15OUT	T15CAP	–	MISO0	EC15	–	–	–
PB5	T21OUT	T21CAP	–	MOSI0	–	–	–	–
PB6	T11OUT	T11CAP	TXD11	MOSI11	EC11	SCL0	–	–
PB7	T12OUT	T12CAP	RXD11	MISO11	EC12	SDA0	–	–
PB8	T14OUT	T14CAP	–	SCK11	EC14	SCL0	–	–
PB9	T15OUT	T15CAP	SS1	SS11	EC15	SDA0	–	–
PB10	T20OUT	T20CAP	TXD12	MOSI12	–	SCL1	SCK1	–
PB11	T20OUT	T20CAP	RXD12	MISO12	–	SDA1	–	–
PB12	T14OUT	T14CAP	SS1	SCK12	EC14	–	–	–
PB13	T21OUT	T21CAP	–	SCK1	–	SCL1	–	–
PB14	T10OUT	T10CAP	SS12	MISO1	EC10	SDA1	–	–
PB15	T10OUT	T10CAP	–	MOSI1	EC10	ADTRG	–	–

**Table 9. GPIO alternate functions (continued)**

Pin Name	Alternate Function							
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	–	–	–	–	–	AN10	–	–
PC1	–	–	–	–	–	AN11	–	–
PC2	–	–	–	MISO1	–	AN12	–	–
PC3	T13OUT	T13CAP	–	MOSI1	EC13	AN13	–	–
PC4	–	–	TXD12	MOSI12	–	AN14	–	–
PC5	T21OUT	T21CAP	RXD12	MISO12	–	AN15	–	–
PC6	T21OUT	T21CAP	–	–	–	–	–	–
PC7	T11OUT	T11CAP	–	–	EC11	–	–	–
PC8	T12OUT	T12CAP	–	–	EC12	–	–	–
PC9	–	–	–	–	–	ADTRG	–	–
PC10	–	–	TXD12	MOSI12	–	TXD13	MOSI13	–
PC11	–	–	RXD12	MISO12	EC21	RXD13	MISO13	–
PC12	–	–	–	SCK12	–	–	SCK13	–
PC13	–	RTCOUT	–	–	–	–	–	–
PC14	SXIN	–	–	–	–	–	–	–
PC15	SXOUT	–	–	–	–	–	–	–
PD2	–	–	–	–	–	SCL2	–	–
PD3	–	–	–	–	–	SDA2	–	–
PD4	–	–	–	SCK13	CLKO	–	–	–
PD5	BOOT	RTCOUT	–	–	CLKO	CMUSYNC	–	–
PF0	XIN	CLKO	–	–	–	–	–	–
PF1	XOUT	–	–	–	–	–	–	–
PF2	T21OUT	T21CAP	SS12	–	–	–	–	–

## 4. Electrical Characteristics

### 4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to  $V_{SS}$ .

#### 4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency

Data based on characterization results, design simulations, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

#### 4.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 5.0\text{ V}$ . The typical data are provided only as design recommendations and are not tested.

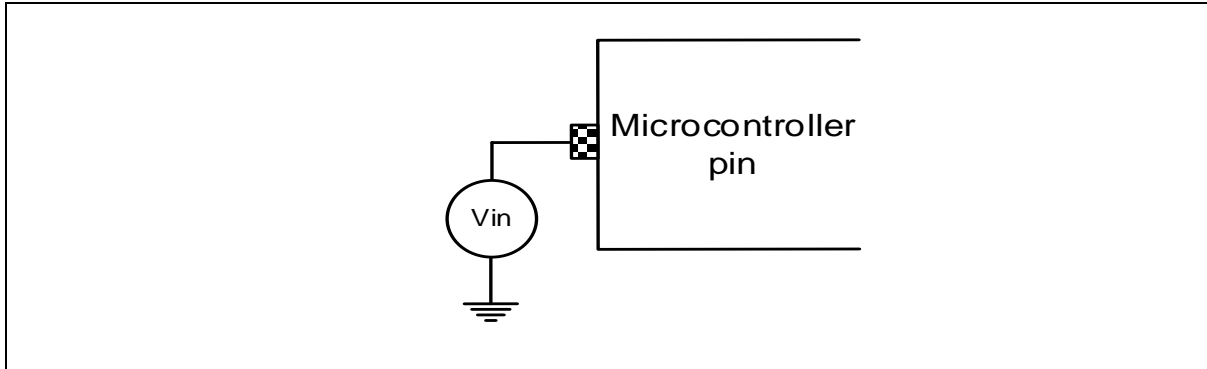
#### 4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

#### 4.1.4 Pin Input Voltage

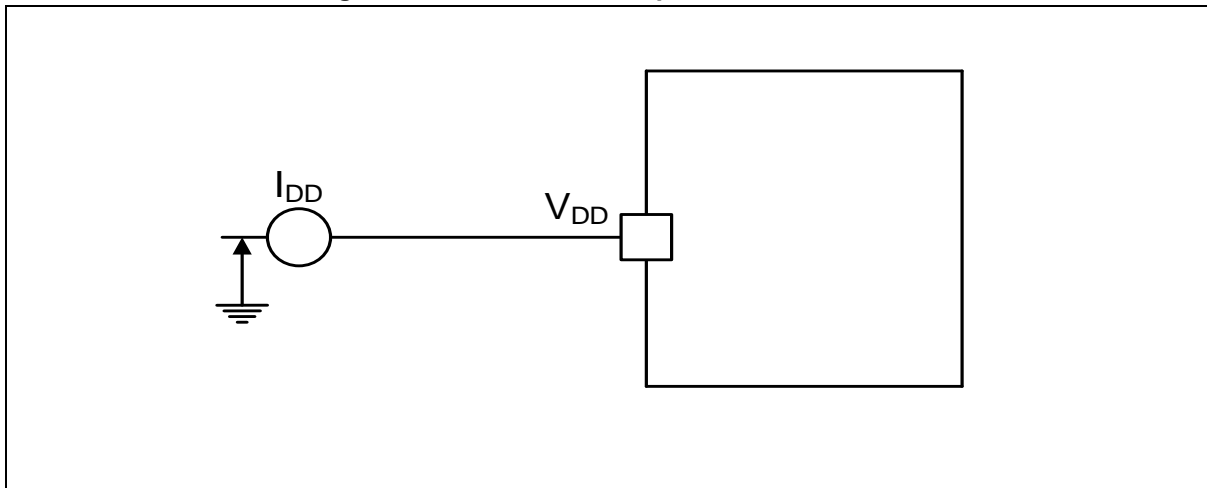
The input voltage measurement on a pin of the device is described in Figure 10.

Figure 10. Pin Input Voltage



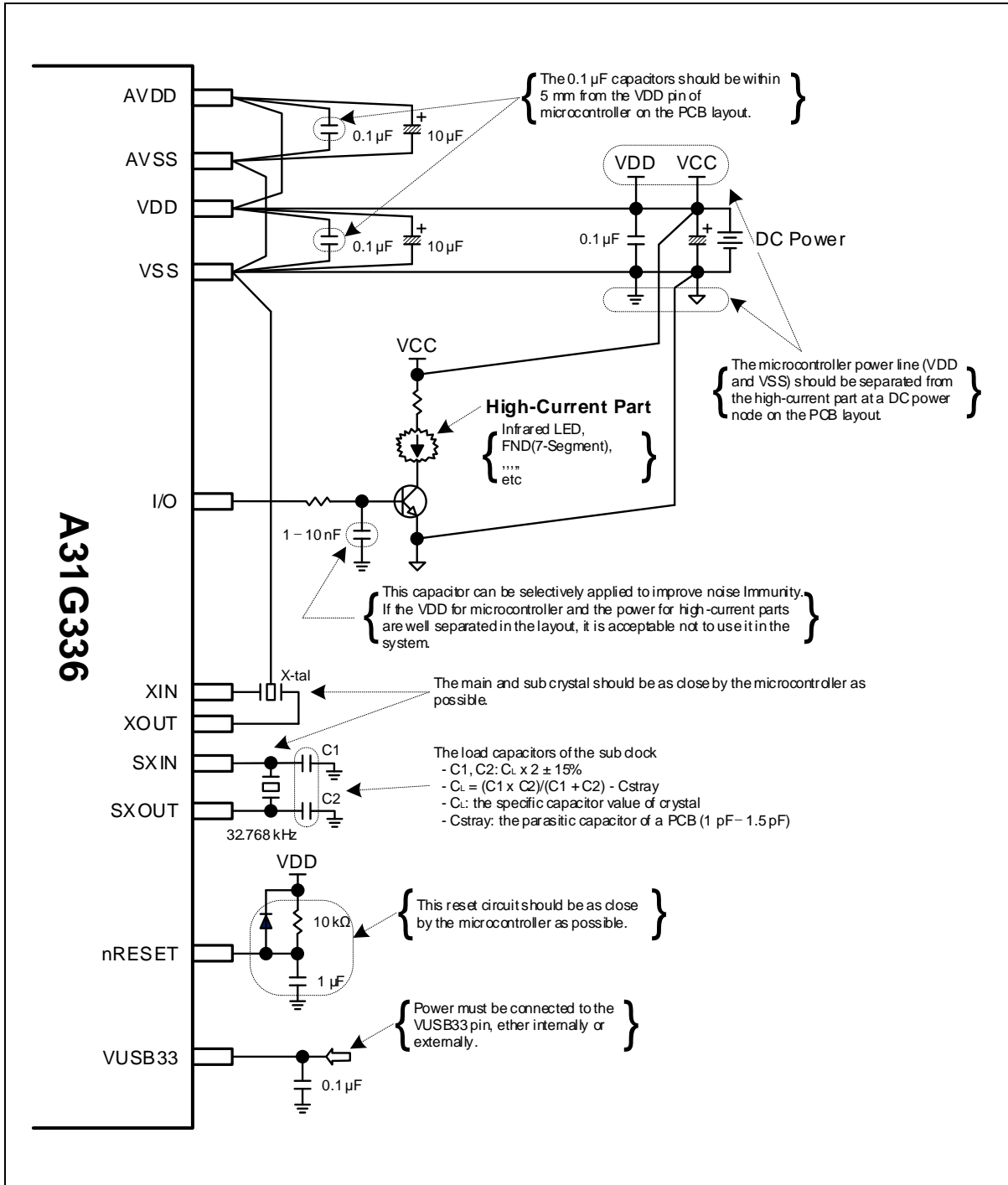
#### 4.1.5 Current Consumption Measurement

Figure 11. Current Consumption Measurement



4.1.6 Power Supply Diagram

Figure 12. Power Supply Diagram



NOTE:

- Each power supply pair (VDD/VSS etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

## 4.2 Absolute Maximum Ratings

Exceeding stresses specified in Table 10 for voltage characteristics, Table 10 for current characteristics, or Table 11 for thermal characteristics may result in permanent damage to the device.

The values listed in the tables are stress ratings only and do not imply that the device will function correctly under these conditions. Prolonged exposure to these maximum rating conditions may impact on the device's reliability.

It is important to operate the device within its specified maximum ratings to ensure reliable performance.

**Table 10. Voltage Characteristics**

Symbol	Description	Min.	Max.	Unit
$V_{DD} - V_{SS}^{(1)}$	External main supply voltage (including $V_{DD}$ )	-0.3	6.5	V
$V_I$	Input voltage on I/O	-0.3	Max. ( $V_{DD}$ ) + 0.3	V
$V_O$	Output voltage on I/O	-0.3	Max. ( $V_{DD}$ ) + 0.3	V

**NOTES:**

1. All main power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) pins must always be connected to the external power supply, in the permitted range.
2.  $V_I$  maximum must always be respected.

**Table 11. Current Characteristics**

Symbol	Description	Max.	Unit
$\Sigma I_{VDD}$	Total current flowing into all $V_{DD}$ power lines (source) <sup>(1)</sup>	120	mA
$\Sigma I_{VSS}$	Total current flowing out of all $V_{SS}$ ground lines (sink) <sup>(2)</sup>	120	mA
$I_{OH}$	Maximum out current sourced by any I/O and control pin	-25	mA
$\Sigma I_{OH(PIN)}$	Total output current sourced by sum of all I/Os and control pins <sup>(2)</sup>	-100	mA
$I_{OL(PIN)}$	Maximum output current sunk by any I/O and control pin	25	mA
$\Sigma I_{OL(PIN)}$	Total output current sunk by sum of all I/Os and control pins <sup>(2)</sup>	100	mA
$P_T$	Total power dissipation	300	mW

**NOTES:**

1. All main power ( $V_{DD}$ ) and ground ( $V_{SS}$ ) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

**Table 12. Thermal Characteristics**

Symbol	Description	Value	Unit
$T_{OP}$	Operating temperature (commercial grade)	-40 to 85	°C
$T_{STG}$	Storage temperature range	-65 to 125	°C
$T_J$	Maximum junction temperature	125	°C

## 4.3 Operating Conditions

### 4.3.1 Recommended Operating Conditions

**Table 13. Recommended Operating Conditions**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage	-	1.8 <sup>(1)</sup>	-	5.5	V
FREQ	Operating frequency	HSI @ 1.8 ≤ VDD ≤ 5.5	2.0	-	32	MHz
		LSI @ 1.8 ≤ VDD ≤ 5.5	-	40	-	kHz
		External clock @ 3.0 ≤ VDD ≤ 5.5	2.0	-	48	MHz
		Main oscillator (ceramic) @ 2.0 ≤ VDD ≤ 5.5	2.0	-	4.2	MHz
		Main oscillator (crystal) @ 2.7 ≤ VDD ≤ 5.5	2.0	-	16	MHz
		PLL @ 1.8 ≤ VDD ≤ 5.5	4.0	-	48	MHz
		Sub-oscillator @ 2.7 ≤ VDD ≤ 5.5	32	-	38	kHz
V <sub>IN</sub>	I/O input voltage	-	-0.3	-	V <sub>DD</sub>	V
T <sub>A</sub>	Ambient temperature	Commercial @ 1.8 ≤ VDD ≤ 5.5	-40	-	85	°C
T <sub>J</sub>	Junction temperature	-	-40	-	105	°C

**NOTE:**

1. When RESET is released, functionality is guaranteed down to VLVR Min.

### 4.3.2 Power-On Reset Characteristics

**Table 14. Power-On Reset Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I <sub>DD</sub>	Operating current	-	-	0.1	-	μA
V <sub>set</sub>	POR setting level	-	-	1.4	-	V
t <sub>R</sub>	V <sub>DD</sub> voltage rising time	0.2 V to 2.0 V	0.01	-	20	ms/V
t <sub>F</sub>	V <sub>DD</sub> voltage falling time	0.2 V to 2.0 V	0.01	-	20	ms/V
V <sub>reset</sub>	POR reset level	-	-	1.0	-	V
ΔV	Hysteresis voltage	-	-	0.2	-	V

### 4.3.3 Reset and Power Control Block Characteristics (LVR and LVI)

The parameters listed in Table 15 and Table 16 are obtained through tests conducted under ambient temperature conditions, which are specified in Table 13.

**Table 15. Low Voltage Reset Characteristics**

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
$V_{LVR\_R}^{(1)}$	LVR Rising edge threshold	LVRVS[3:0]		1111	–	1.68	1.79
$V_{LVR\_F}^{(1)}$	LVR falling edge threshold	LVRVS[3:0]		1100	1.80	1.93	2.06
				1011	1.86	2.00	2.14
				1010	1.98	2.13	2.28
				1001	2.15	2.31	2.47
				1000	2.31	2.48	2.65
				0111	2.49	2.68	2.87
				0110	2.84	3.05	3.26
				0101	2.97	3.19	3.41
				0100	3.35	3.60	3.85
				0011	3.48	3.74	4.00
				0010	3.76	4.04	4.32
				0001	3.93	4.22	4.51
0000	4.19	4.50	4.81				
$\Delta V$	Hysteresis	–		–	100	200	mV
$t_{LVRW}$	Minimum pulse width	–		100	–	–	$\mu s$
–	Noise cancelling time	–		–	2	–	$\mu s$
$I_{LVR}$	LVR current	Enable	$V_{DD} = 5 V$	–	3.5	5.0	$\mu A$
		Disable		–	–	0.1	

**NOTE:**

1. The LVR threshold is selected by LVRVS[3:0] bits of CONF\_LVRCNFIG register in the Configure Option Area.

Table 16. Low Voltage Indicator Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
$V_{LVI\_F}^{(1)(2)}$	Detection level	Falling edge voltage		1.80	1.93	2.06	V
				1.86	2.00	2.14	
				1.98	2.13	2.28	
				2.15	2.31	2.47	
				2.31	2.48	2.65	
				2.49	2.68	2.87	
				2.84	3.05	3.26	
				2.97	3.19	3.41	
				3.35	3.60	3.85	
				3.48	3.74	4.00	
				3.76	4.04	4.32	
				3.93	4.22	4.51	
				4.19	4.50	4.81	
$\Delta V$	Hysteresis	–		–	100	200	mV
$t_{LVRW}$	Minimum pulse width	–		100	–	–	$\mu s$
–	Noise cancelling time	–		–	2	–	$\mu s$
$I_{LVI}$	LVI current	Enable	$V_{DD} = 5 V$	–	3.5	5.0	$\mu A$
		Disable		–	–	0.1	

**NOTES:**

1. The LVI level can be selected by the SCU\_LVICR.LVIVS[3:0] bits.
2. Refer to the low voltage indicator control register of chapter 4.8.25 in the user's manual.

#### 4.3.4 Current Consumption Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 17.

##### 4.3.4.1 Supply Voltage and Current Consumption

**Table 17. Supply Voltage and Current Characteristics**

Symbol	Parameter	Condition	Typ.	Max.	Unit	
I <sub>DD1</sub> (Main RUN)	Supply current	f <sub>HSI</sub> = 32 MHz	V <sub>DD</sub> = 5V ± 10%	4.5	9.0	mA
		f <sub>HSI</sub> = 16 MHz	V <sub>DD</sub> = 5V ± 10%	3.0	6.0	
		f <sub>HSI</sub> = 8 MHz	V <sub>DD</sub> = 5V ± 10%	1.9	3.8	
		f <sub>HSE</sub> = 16 MHz	V <sub>DD</sub> = 5V ± 10%	3.5	7.0	
			V <sub>DD</sub> = 3V ± 10%	2.7	5.4	
		f <sub>HSE</sub> = 8 MHz	V <sub>DD</sub> = 5V ± 10%	2.2	4.4	
f <sub>PLL</sub> = 48 MHz	V <sub>DD</sub> = 5V ± 10%	6.0	12.0			
I <sub>DD2</sub> (Main SLEEP)	Supply current	f <sub>HSI</sub> = 32 MHz	V <sub>DD</sub> = 5V ± 10%	2.3	4.6	mA
		f <sub>HSI</sub> = 16 MHz	V <sub>DD</sub> = 5V ± 10%	1.5	3.0	
		f <sub>HSI</sub> = 8 MHz	V <sub>DD</sub> = 5V ± 10%	1.2	2.4	
		f <sub>HSE</sub> = 16 MHz	V <sub>DD</sub> = 5V ± 10%	2.0	4.0	
			V <sub>DD</sub> = 3V ± 10%	1.3	2.6	
		f <sub>HSE</sub> = 8 MHz	V <sub>DD</sub> = 5V ± 10%	1.4	2.8	
f <sub>PLL</sub> = 48 MHz	V <sub>DD</sub> = 5V ± 10%	3.5	7.0			
I <sub>DD3</sub> (Sub-RUN)	Supply current	f <sub>LSE</sub> = 32.768 kHz or f <sub>LSI</sub> = 40 kHz		35.0	70.0	μA
I <sub>DD4</sub> (Sub-SLEEP)		V <sub>DD</sub> = 3V/5V ± 10%, T <sub>A</sub> = 25°C		6.0	12.0	μA
I <sub>DD5</sub> (DEEP-SLEEP)		RTCC/f <sub>LSE</sub> off	V <sub>DD</sub> = 5V ± 10%, T <sub>A</sub> = 25°C	1.5	5.0	μA
		RTCC/f <sub>LSE</sub> on		3.5	8.0	

**NOTES:**

1. Where the f<sub>HSE</sub> is an external main oscillator, the f<sub>LSE</sub> is an external sub-oscillator, and the f<sub>HSI</sub> is a high frequency internal RC oscillator, the f<sub>LSI</sub> is a low-speed internal RC oscillator, and the fx is the selected system clock.
2. All supply current items do not include the current of the low-speed internal RC (LSI) oscillator and peripheral blocks. However, they include the current of the Power-on Reset (POR) block.
3. Each current consumption is measured as 0-wait for 20 MHz or less, 1-wait for 32 MHz, and 2-wait for 48 MHz.

#### 4.3.4.2 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

#### 4.3.4.3 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be simply calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

To estimate the current consumption for output pins, any external pull-down or load must also be taken into consideration.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. Therefore, it is recommended to avoid applying an intermediate voltage level if there is no specific need for this configuration.

#### 4.3.4.4 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

### 4.3.5 External Clock Source Characteristics

#### 4.3.5.1 External Main Oscillator

The external main oscillator (HSE) clock can be generated using a crystal/ceramic resonator oscillator with a frequency range of 2 to 16 MHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 18.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

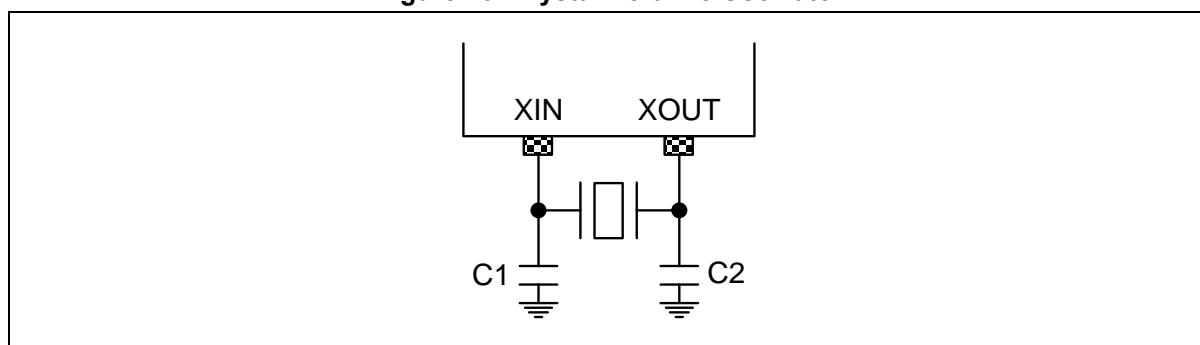
**Table 18. External Main Oscillator Characteristics <sup>(1)</sup>**

Symbol	Parameter	Condition <sup>(2)</sup>	Min.	Typ.	Max.	Unit
$f_{HSE}$	HSE crystal frequency	$V_{DD} = 2.7\text{ V to }5.5\text{ V}$	2.0	–	16.0	MHz
	HSE ceramic oscillator frequency	$V_{DD} = 2.0\text{ V to }5.5\text{ V}$	2.0	–	4.2	
		$V_{DD} = 2.7\text{ V to }5.5\text{ V}$	2.0	–	16.0	
$f_{OSC\_IN}$	XIN input frequency	$V_{DD} = 3.0\text{ V to }5.5\text{ V}$	2.0	–	48.0	MHz
	External clock duty ratio	–	–	50	–	%
$R_F$	Feedback resistor	$XIN = V_{DD}$ , $XOUT = V_{SS}$ , $T_A = 25^\circ\text{C}$ , $V_{DD} = 5\text{ V}$	0.7	1.0	1.3	M $\Omega$
$t_{SU(HSE)}^{(3)}$	HSE crystal startup time	$V_{DD} = 2.7\text{ V to }5.5\text{ V}$ , $f_{HSE} \geq 2\text{ MHz}$	–	–	60	ms
	HSE ceramic oscillator startup time	$V_{DD} = 2.0\text{ V to }5.5\text{ V}$ , $4.2\text{ MHz} \geq f_{HSE} \geq 2\text{ MHz}$	–	–	10	
$t_{XH/XL}$	Duration of high or low state of XIN input	$f_{OSC\_IN} = 2.0\text{ to }48\text{ MHz}$	10.4	–	250	ns

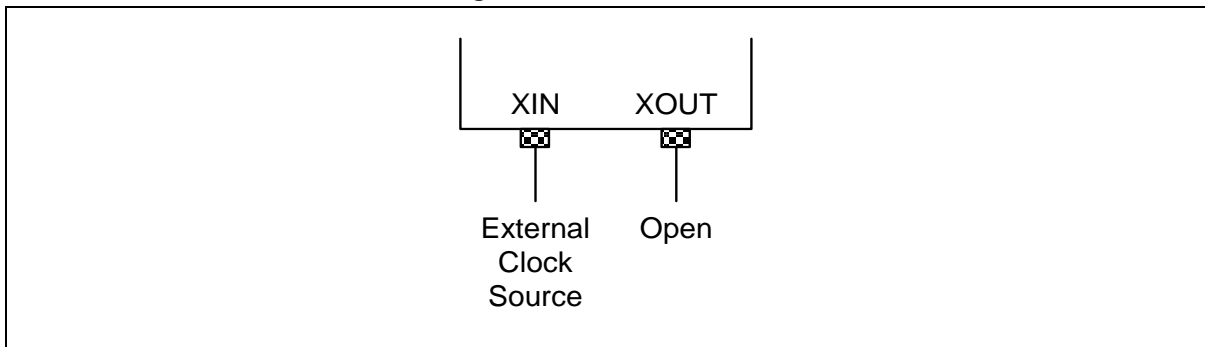
**NOTES:**

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3.  $t_{SU(HSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 2 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

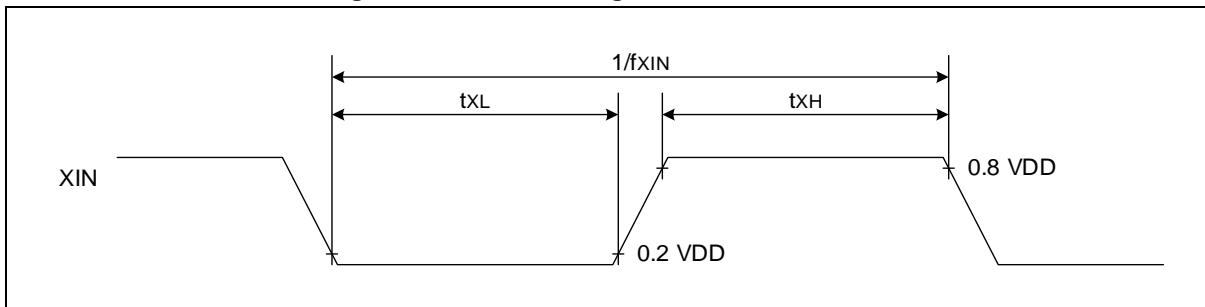
**Figure 13. Crystal/Ceramic Oscillator**



**Figure 14. External Clock**



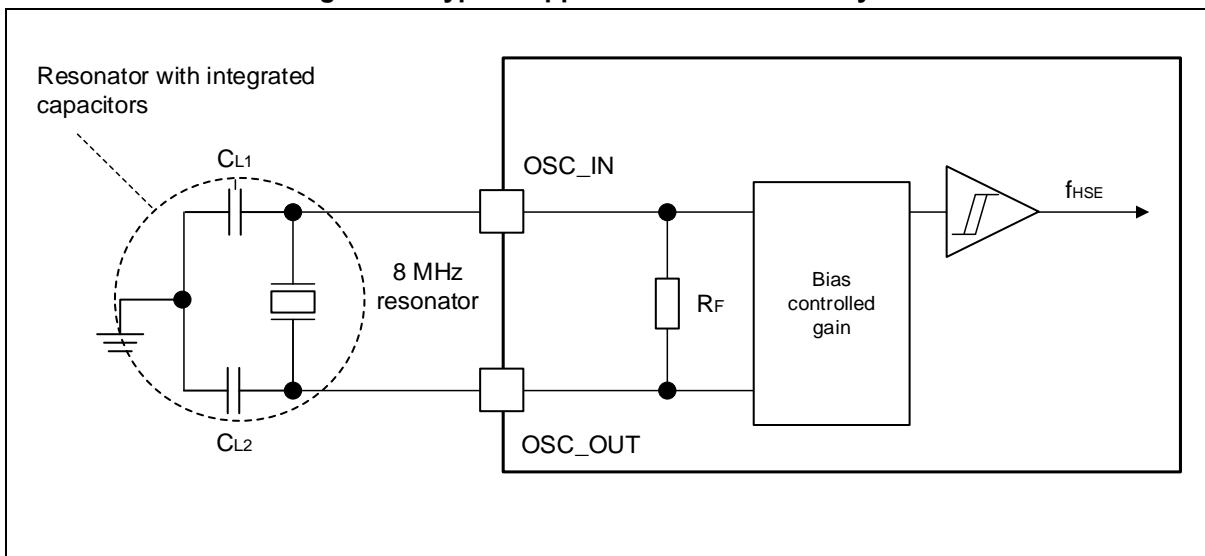
**Figure 15. Clock Timing Measurement at XIN**



It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The CL1 and CL2 capacitors are usually of the same size, and the crystal manufacturer typically specifies a load capacitance that is the series combination of both capacitors. The capacitance values of the CL1 and CL2 capacitors should be set by considering the parasitic capacitance of the printed circuit board (PCB) and microcontroller pins, which is approximately twice the specified load capacitance of the crystal.

Figure 16 shows a circuit diagram of a typical application with an 8 MHz crystal.

**Figure 16. Typical Application With 8 MHz Crystal**



### 4.3.5.2 External Sub-Oscillator

The external sub-oscillator (LSE) clock can be generated using a crystal/ceramic resonator oscillator with a frequency of 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 19.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

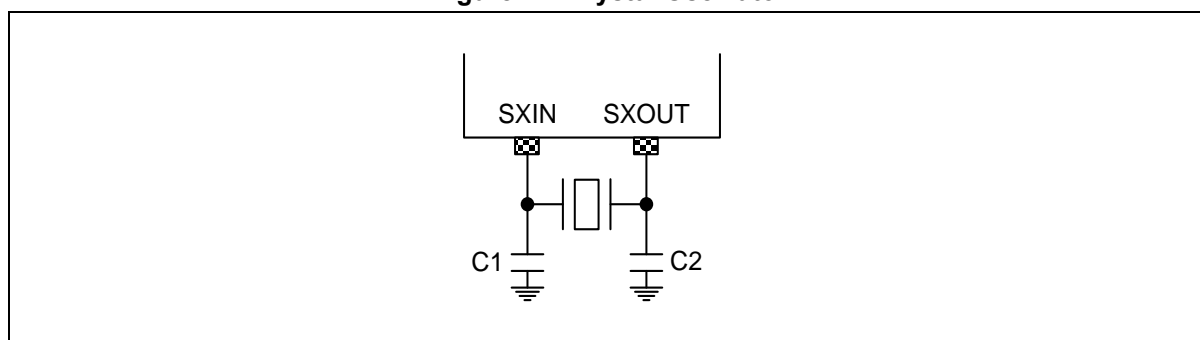
**Table 19. External Sub-Oscillator Characteristics <sup>(1)</sup>**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$f_{LSE}$	LSE oscillator frequency	2.7 V to 5.5 V	32	32.768	38	kHz
$f_{OSC\_SXIN}$	SXIN input frequency	2.7 V to 5.5 V	32	–	38	kHz
$R_F$	Feedback resistor	$T_A = 25^\circ\text{C}$ , $V_{DD} = 5\text{ V}$	6.5	13	26	$M\Omega$
$t_{SU(LSE)}^{(2)}$	LSE crystal startup time	–	–	–	10	s
		$V_{DD} = 3\text{ V}$ , $T_A = 25^\circ\text{C}$		0.7	1.5	
$t_{XH/XL}$	Duration of high or low state of SXIN input	–	13	–	15	$\mu\text{s}$

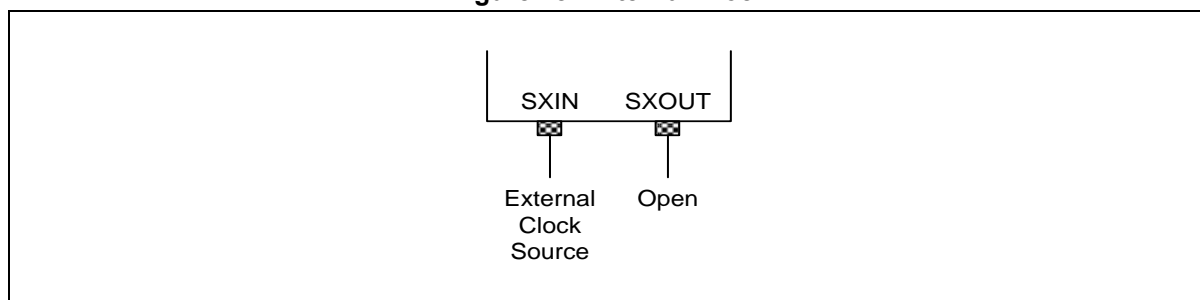
**NOTES:**

1. Guaranteed by design.
2.  $t_{SU}$  (LSI) is the startup time measured from the moment it is enabled (by software) until it reaches a stabilized 32.768 kHz oscillation. This value is measured using a standard crystal resonator and can vary significantly depending on the crystal manufacturer.

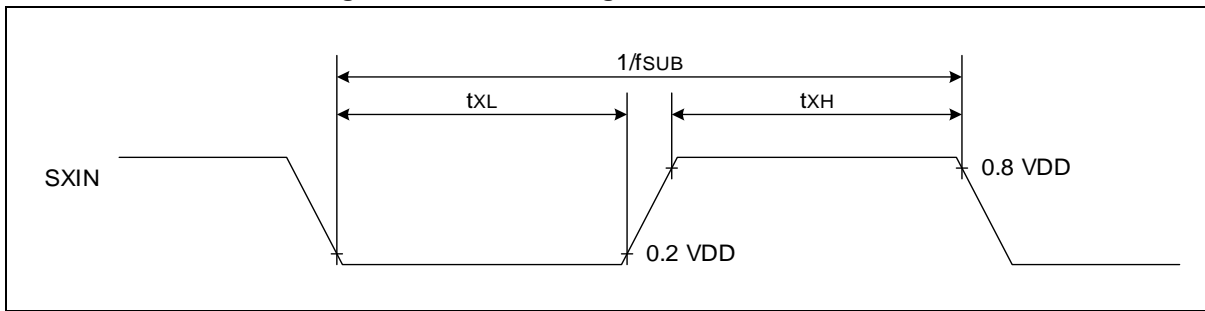
**Figure 17. Crystal Oscillator**



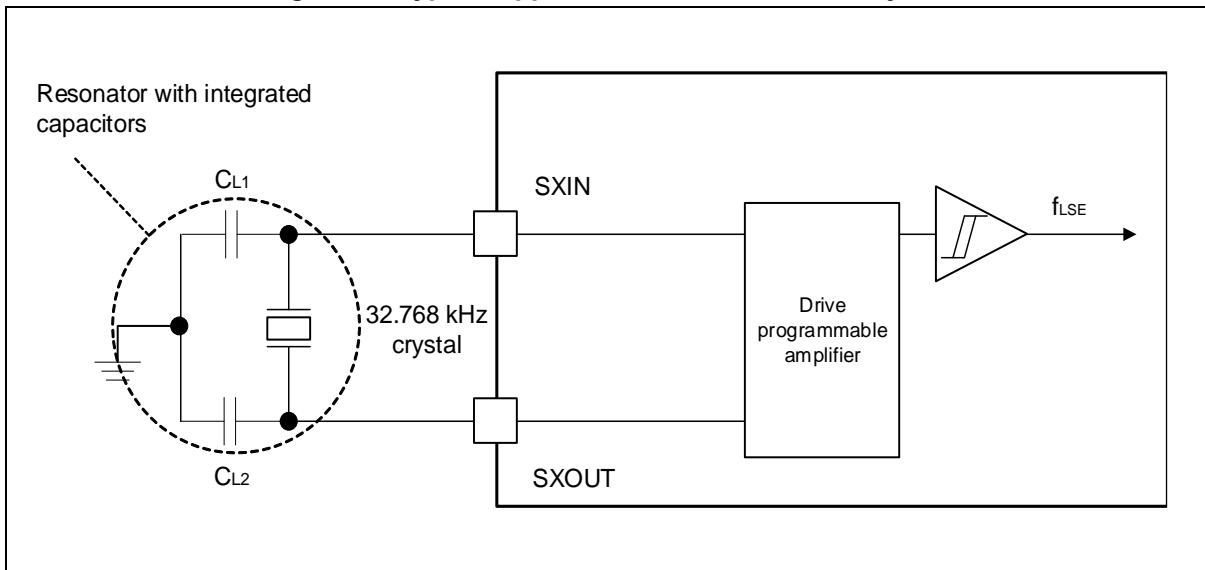
**Figure 18. External Clock**



**Figure 19. Clock Timing Measurement at SXIN**



**Figure 20. Typical Application With 32.768 kHz Crystal**



**NOTE:**

1. An external resistor is not required between SXIN and SXOUT and it is forbidden to add one.

#### 4.3.6 Internal Clock Source Characteristics

The parameters listed in Table 20 and Table 21 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

##### 4.3.6.1 High-Speed Internal RC Oscillator

**Table 20. High-Speed Internal RC Oscillator Characteristics**

Symbol	Parameter	Condition <sup>(2)</sup>	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating voltage	–	1.8	–	5.5	V
f <sub>HSI</sub>	HSI frequency	–	–	32	–	MHz
ACC <sub>HSI</sub> <sup>(1)</sup>	Accuracy	T <sub>A</sub> = 0°C to 50°C	–	–	±1.5	%
		T <sub>A</sub> = –40°C to 85°C (commercial)	–	–	±3.0	
DuCy	Duty cycle	–	40	50	60	%
t <sub>STAB(HSI)</sub>	HSI oscillator stabilization time	–	–	–	2	μs
I <sub>HSI</sub>	HSI oscillator power consumption	HSI oscillator is enabled.	–	500	700	μA
		HSI oscillator is disabled.	–	–	0.1	

**NOTES:**

1. Guaranteed by design, but it may require on-board programming after the SMT process. Calibration of the HSI at high temperatures can result in frequency shifts, so it is important to ensure sufficient calibration time for cooling to near room temperature after the SMT process.

##### 4.3.6.2 Low-Speed Internal RC Oscillator

**Table 21. Low-Speed Internal RC Oscillator Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f <sub>LSI</sub>	LSI frequency	–	34	40	46	kHz
t <sub>STAB(LSI)</sub>	LSI stabilization time	–	–	100	1000	μs
I <sub>LSI</sub>	LSI power consumption	LSI is enabled.	–	2	4	μA
		LSI is disabled.	–	–	0.1	

## 4.3.7 PLL Electrical Characteristics

Table 22. PLL Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f <sub>PLLIN</sub>	Input Frequency Range	–	1	2	3	MHz
f <sub>VCO</sub>	VCO Frequency Range	–	60	–	96	MHz
f <sub>PLL</sub>	Output Frequency Range	–	4	–	48	MHz
T <sub>OD</sub>	Clock Duty Ratio	–	40	50	60	%
t <sub>LOCK</sub>	Locking Time	–	–	–	200	μs
I <sub>PLL</sub>	PLL Current	PLL is enabled.	–	300	500	μA
		PLL is disabled.	–	–	0.1	μA

## 4.3.8 Flash Memory Characteristics

Table 23. Flash Memory Characteristics

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
t <sub>FW</sub>	Write time	Flash write mode		–	25	–	μs
t <sub>FSE</sub>	Page/Sector erase time	–		–	2	–	ms
t <sub>FCE</sub>	Chip erase time	–		–	8	–	ms
V <sub>PGM</sub>	Programming voltage	During erase/write		1.8	–	5.5	V
f <sub>HCLK</sub>	System clock frequency	–		2.0	–	–	MHz
N <sub>FWE</sub>	Endurance of code Flash memory (write/erase operation)	Page 0 to 511 Configuration option page 1	T <sub>A</sub> = 25°C Page unit	10,000	–	–	cycles
		Configuration option page 2/3/4/5		100,000	–	–	
t <sub>FRT</sub>	Retention time	–		10	–	–	years

### 4.3.9 I/O Port Characteristics

The parameters listed in Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

**Table 24. DC Electrical Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
V <sub>IH</sub>	Input high voltage	All input ports, nRESET	0.8 × V <sub>DD</sub>	–	V <sub>DD</sub>	V	
V <sub>IL</sub>	Input low voltage	All input ports, nRESET	–	–	0.2 × V <sub>DD</sub>	V	
V <sub>OH</sub>	Output high voltage	V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = –10 mA, All output ports, T <sub>A</sub> = 25°C	V <sub>DD</sub> – 1.3	–	–	V	
V <sub>OL</sub>	Output low voltage	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 15 mA, All output ports, T <sub>A</sub> = 25°C	–	–	1.3	V	
I <sub>IH</sub>	Input high leakage current	All input ports	–	–	1	μA	
I <sub>IL</sub>	Input low leakage current	All input ports	–1	–	–	μA	
R <sub>PU</sub>	Pull-up resistor	V <sub>I</sub> = 0 V, T <sub>A</sub> = 25°C All input ports	V <sub>DD</sub> = 5 V	25	50	100	kΩ
			V <sub>DD</sub> = 3 V	50	100	200	
		V <sub>I</sub> = 0 V, T <sub>A</sub> = 25°C nRESET	V <sub>DD</sub> = 5 V	150	250	400	
			V <sub>DD</sub> = 3 V				
R <sub>PD</sub>	Pull-down resistor	V <sub>I</sub> = V <sub>DD</sub> , T <sub>A</sub> = 25°C All input ports	V <sub>DD</sub> = 5 V	25	50	100	kΩ
			V <sub>DD</sub> = 3 V	50	100	200	
C <sub>IO</sub>	I/O pin capacitance	F = 1 MHz. Unmeasured pins are connected to V <sub>SS</sub> .	–	–	10	pF	

#### 4.3.9.1 Output Driving Current

The GPIOs are capable of sinking or sourcing currents within the range specified by I<sub>OL</sub> and I<sub>OH</sub>.

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on V<sub>DD</sub> and the maximum operating current of the microcontroller on V<sub>DD</sub> (during RUN mode) must not exceed the absolute maximum rating ΣI<sub>VDD</sub> specified in Table 11.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during RUN mode) must not exceed the absolute maximum rating ΣI<sub>VSS</sub> specified in Table 11.

#### 4.3.9.2 Output Voltage Characteristics

Unless otherwise specified, the parameters in Table 25 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

**Table 25. Output Voltage Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOH	Output high level voltage for an I/O pin	VDD = 4.5 V, IOH = -10 mA	VDD - 1.3	-	-	V
VOL	Output low level voltage for an I/O pin	VDD = 4.5 V, IOL = 15 mA	-	-	1.3	V

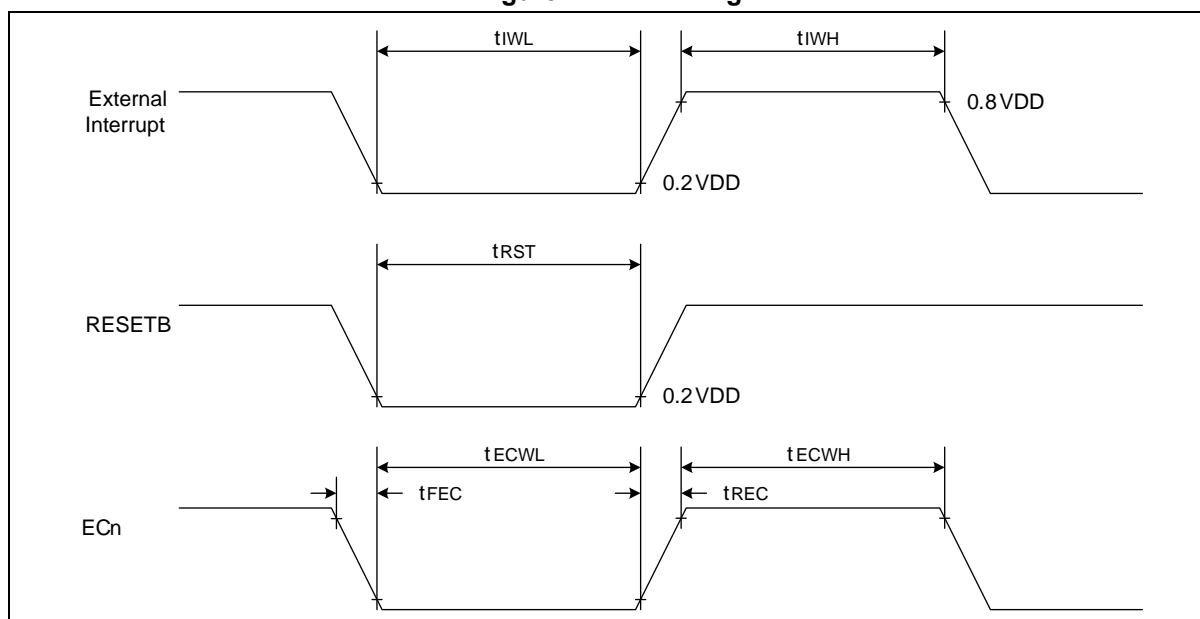
4.3.9.3 AC Characteristics

Unless otherwise specified, the parameters in Table 26 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

Table 26. AC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{RST}$	RESETB input low width	$V_{DD} = 5\text{ V}$	10	–	–	$\mu\text{s}$
$t_{IWH}, t_{IWL}$	Interrupt input high, low width	$V_{DD} = 5\text{ V}$ , all interrupts	100	–	–	ns
$t_{ECWH}, t_{ECWL}$	External counter input high, low pulse width	$V_{DD} = 5\text{ V}$ , all external counter inputs	100	–	–	ns
$t_{REC}, t_{FEC}$	External counter transition time	$V_{DD} = 5\text{ V}$ , all external counter inputs	–	–	20	ns
$f_{IO1}$	I/O frequency	$V_{DD} = 5.0\text{ V}$ , $C_L = 30\text{ pF}$ All except $f_{IO2}$	–	–	6	MHz
$f_{IO2}$		$V_{DD} = 2.7\text{ V}$ , $C_L = 30\text{ pF}$ , SPI pins	–	–	8	MHz

Figure 21. AC Timing



### 4.3.10 Analog-to-Digital Converter Characteristics

Unless otherwise specified, the parameters in Table 27 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

**Table 27. ADC Electrical Characteristics**

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Operating voltage	–		2.7	–	5.5	V
–	Resolution	–		–	12	–	bit
V <sub>AN</sub>	Analog input voltage	–		AV <sub>SS</sub>	–	AV <sub>DD</sub>	V
AV <sub>DD</sub>	Analog voltage	–		V <sub>DD</sub> -0.3	V <sub>DD</sub>	V <sub>DD</sub> +0.3	V
V <sub>ADCBUF</sub>	Band Gap Reference Buffer Voltage	–		900	950	1000	mV
I <sub>ADC</sub>	ADC current	ADC is enabled.	AV <sub>DD</sub> = 5.0 V f <sub>ADC</sub> = 24 MHz	–	1.6	–	mA
		ADC is disabled.		–	–	0.1	μA
I <sub>AN</sub>	ADC input leakage current	AV <sub>DD</sub> = 5.0 V		–	–	2	μA
t <sub>CONV</sub>	Conversion time	3.0 V < AV <sub>DD</sub>		1	–	–	μs
		2.7 V < AV <sub>DD</sub>		2	–	–	
f <sub>ADC</sub>	Operating frequency	–		–	–	25	MHz
INL	Integral non-linearity	–		–	±3	±6	LSB
DNL	Differential non-linearity			–	±2	±3	
ZOE <sup>(1)</sup>	Zero-offset error			–	±4	–	
FSE <sup>(2)</sup>	Full-scale error			–	±4	–	

**NOTES:**

1. The zero offset error is the discrepancy between the value of 0x000 and the converted output value when a zero-input voltage (AV<sub>SS</sub>) is applied.
2. The full-scale error is the discrepancy between the value of 0xFFFF and the converted output value when the full-scale voltage (AV<sub>DD</sub>) is applied.
3. T<sub>A</sub> = 25°C

#### 4.3.10.1 General PCB Design Guidelines

The power supply must be separated in accordance with the scheme shown in Figure 12. The decoupling capacitors across the V<sub>DD</sub>/AV<sub>DD</sub> are ceramic (good quality) capacitors and must be placed as close as possible to the chip.

### 4.3.11 Comparator Characteristics

Unless otherwise specified, the parameters in Table 28 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 13.

**Table 28. Comparator Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{OF}$	Offset Error	–	–	±5	±10	mV
		Using internal VREF	–	±20	±70	
$V_{HYS(None)}$	Hysteresis	–	–	0	–	mV
$V_{HYS(Low)}$		High Speed Mode	–	15	40	
		Other Modes	–	10	25	
$V_{HYS(Mid)}$		High Speed Mode	–	50	125	
		Other Modes	–	20	50	
$V_{HYS(High)}$		High Speed Mode	–	150	400	
	Other Modes	–	30	75		
$t_{DELAY}$	Propagation Delay for 200mV Step with 100mV Overdrive	Ultra-low Power Mode	–	8	25	µs
		Low Power Mode	–	3.5	12	
		Medium Power Mode	–	2.5	8	
		High Speed Mode $2.7 V \leq V_{DD}$	–	0.7	2.1	
		High Speed Mode $2.0 V \leq V_{DD} < 2.7 V$	–	1.5	4.5	
$t_{DELAY}$	Propagation Delay for Full Range Step with 100mV Overdrive	Ultra-low Power Mode	–	8	25	µs
		Low Power Mode	–	3.5	12	
		Medium Power Mode	–	3	8	
		High Speed Mode $2.7 V \leq V_{DD}$	–	0.7	2.1	
		High Speed Mode $2.0 V \leq V_{DD} < 2.7 V$	–	1.5	4.5	
$I_{CMP}$	Comparator Current	Ultra-low Power Mode, COMP0	–	0.8	1.5	µA
		Ultra-low Power Mode, COMP0/1	–	1.5	–	
		Low Power Mode, COMP0	–	2	5	
		Low Power Mode, COMP0/1	–	3.5	–	
		Medium Power Mode, COMP0	–	5	15	
		Medium Power Mode, COMP0/1	–	10	–	
		High Speed Mode, COMP0	–	25	100	
High Speed Mode, COMP0/1	–	50	–			
$V_{OUT1}$	VREF Output Voltage for Comparators	$2.7 V \leq V_{DD}$	1.14	1.2	1.26	V
$V_{OUT2}$			0.855	0.9	0.945	
$V_{OUT3}$			0.57	0.6	0.63	
$V_{OUT4}$			0.285	0.3	0.315	

**NOTES:**

1.  $T_A = 25^\circ\text{C}$

## 4.3.12 Temperature Sensor Characteristics

Table 29. Temperature Sensor Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
T <sub>LIN</sub>	Temperature Linearity	–	–	±10	–	°C	
ΔF	Frequency Variation	$(F(T2) - F(T1)) \div (T2 - T1)$	1.6	3.6	6.5	kHz/°C	
–	Frequency Deviation	$\Delta F \div F(30)$	0.3	0.45	0.6	%	
I <sub>TS</sub>	Sensor Current	Enable	V <sub>DD</sub> = 5.0 V	–	10	20	μA
		Disable		–	–	10	nA
t <sub>START</sub>	Startup Time	–	–	–	500	μs	

**NOTE:**

1. Temperature =  $\{(F(T) - F(30)) \div \Delta F\} + 30$  [°C]  
Where T1 = 30°C, T2 = 85°C
  - A. F(T1) [kHz] is the temperature sensor output frequency acquired at 30°C.
  - B. F(T2) [kHz] is the temperature sensor output frequency acquired at 85°C.
  - C. F(T) [kHz] is the temperature sensor output frequency acquired at an arbitrary temperature.

**4.3.13 Communication Interface Characteristics**

**4.3.13.1 I2C Interface Characteristics**

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

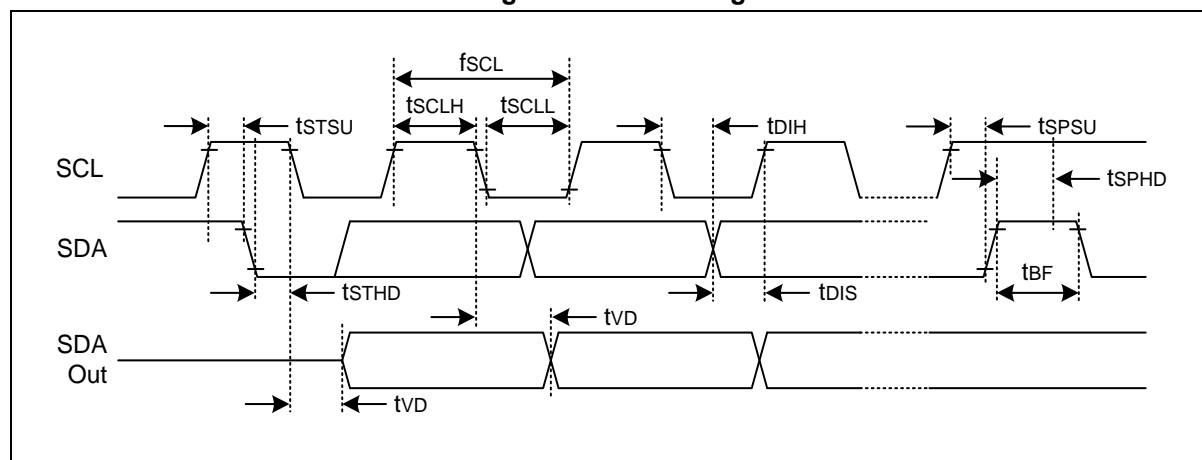
- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate
- Fast mode plus (Fm+): up to 1 Mbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

**Table 30. I2C Characteristics**

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
–	I2C Operating voltage	$V_{DD} \geq 1.8\text{ V}$		$V_{DD} \geq 2.0\text{ V}$		$V_{DD} \geq 2.7\text{ V}$		V
$f_{SCL}$	Clock frequency	0	100	0	400	0	1,000	kHz
$t_{SCLH}$	Clock high pulse width	4.0	–	0.6	–	0.26	–	$\mu\text{s}$
$t_{SCLL}$	Clock low pulse width	4.7	–	1.3	–	0.5	–	
$t_{BF}$	Bus free time	4.7	–	1.3	–	0.5	–	
$t_{STSU}$	Start condition setup time	4.7	–	0.6	–	0.26	–	
$t_{STHD}$	Start condition hold time	4.0	–	0.6	–	0.26	–	
$t_{SPSU}$	Stop condition setup time	4.0	–	0.6	–	0.26	–	
$t_{SPHD}$	Stop condition hold time	4.0	–	0.6	–	0.26	–	
$t_{VD}$	Output valid from clock	0	–	0	–	0	–	
$t_{DIH}$	Data input hold time	0	–	0	1.0	0	0.45	
$t_{DIS}$	Data input setup time	250	–	100	–	50	–	

**Figure 22. I2C Timing**



**4.3.13.2 SPI Interface Characteristics**

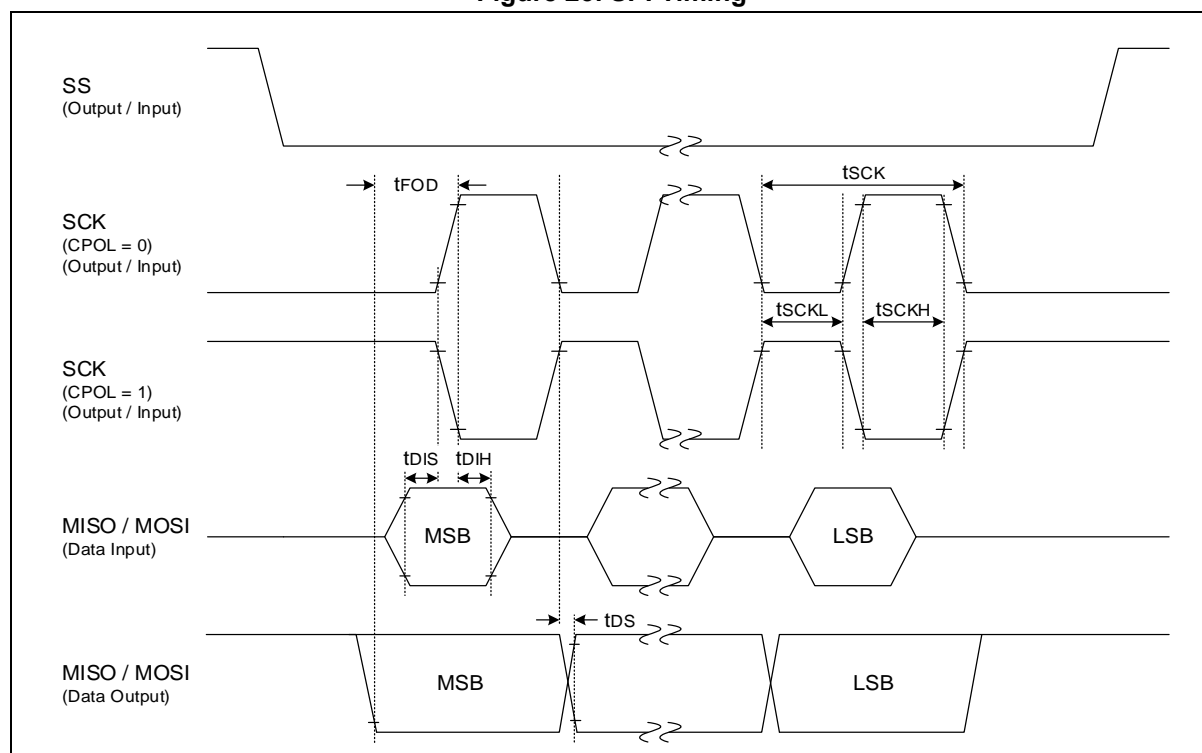
Unless otherwise specified, the parameters in Table 31 are obtained through tests conducted under ambient temperature,  $f_{PCLK}$  frequency and supply voltage conditions, which are specified in Table 13.

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO for SPI), refer to 4.3.9.

**Table 31. SPI Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
$f_{SCK}$	SPI clock frequency	$VDD \geq 2.7\text{ V}$	Internal SCK source	-	-	8	
			External SCK source				
		$VDD \geq 1.8\text{ V}$	Internal SCK source	-	-		4
			External SCK source				
$t_{SCKH}$ , $t_{SCKL}$	Input/output clock high, low pulse width	Internal/External SCK source	$0.8 \times$ Typ.	$t_{SCK}/2$	$1.2 \times$ Typ.	ns	
$t_{FOD}$	First output clock delay time	Internal/External SCK source, CPHA = 0	$0.4 \times$ $t_{SCK}$	-	-	ns	
$t_{DS}$	Output clock delay time	-	-	-	25	ns	
$t_{DIS}$	Input setup time		17	-	-	ns	
$t_{DIH}$	Input hold time		20	-	-	ns	
Duty	Duty cycle of SPI frequency (SCK)	Slave mode	40	50	60	%	

**Figure 23. SPI Timing**



#### 4.3.13.3 UART Interface Characteristics

Unless otherwise specified, the parameters in Table 32 are obtained through tests conducted under ambient temperature,  $f_{CLK}$  frequency and supply voltage conditions, which are specified in Table 13.

**Table 32. UART Characteristic**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$F_{max}$	Maximum character transmission frequency	–	–	0.32	Mbits

#### 4.3.13.4 USB Electrical Characteristics

**Table 33. USB Electrical Characteristic**

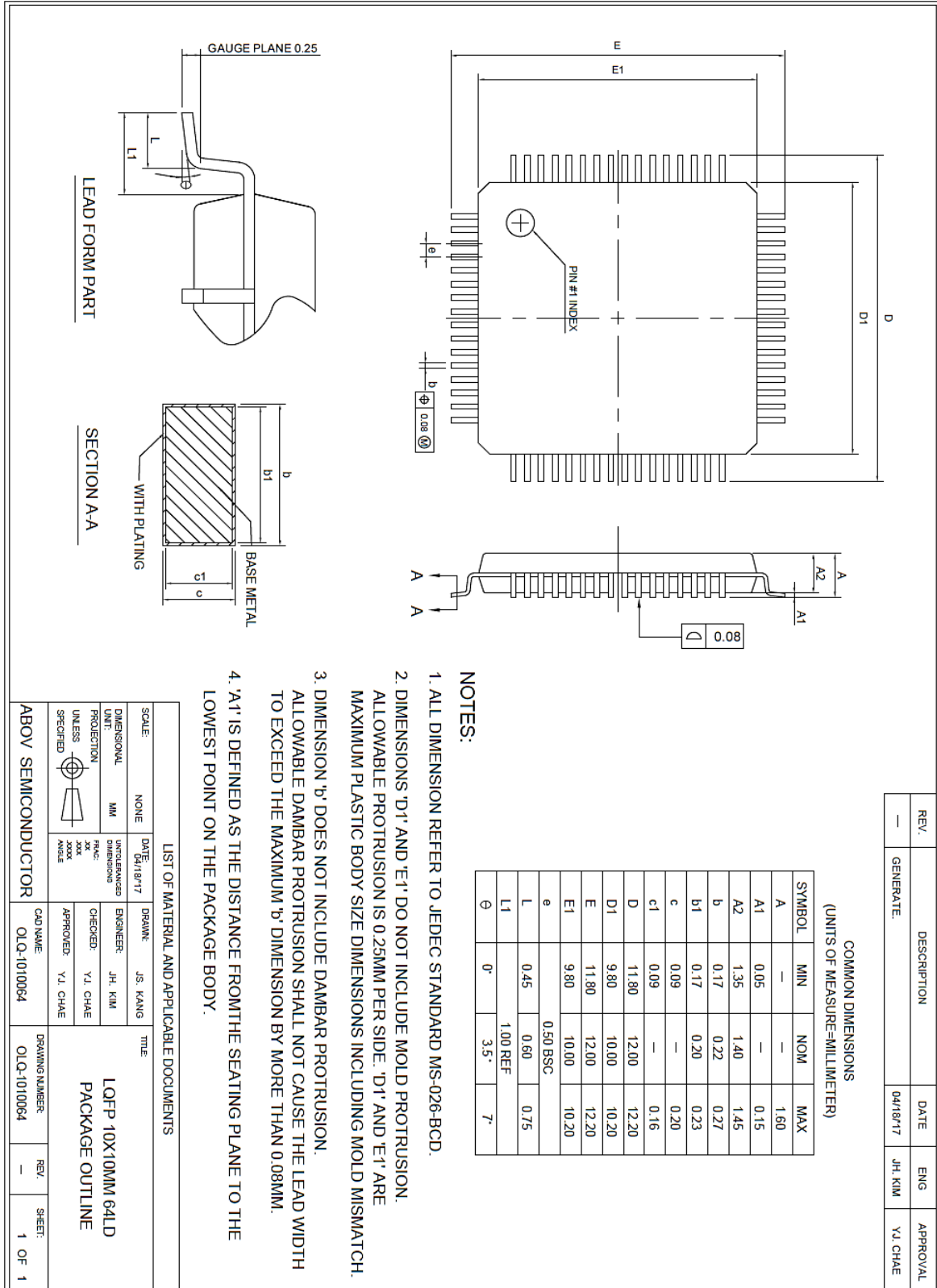
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{DD}$	Operating voltage	–	3.0	–	5.5	V
VUSB33		–	3.0	–	3.6	V
VUSB33	Output Voltage of Internal LDO	$V_{DD} \geq 4.0$ V	3.0	3.3	3.6	V
$R_{PU}$	Pull-up resistor	USBDP, $T_A = 25^\circ\text{C}$	1.425	1.5	1.575	k $\Omega$
		USBDM, $T_A = 25^\circ\text{C}$	-	1.5	-	
$R_{PD}$	Pull-down resistor	USBDM, USBDP $T_A = 25^\circ\text{C}$	-	15	-	k $\Omega$
$V_{DIFFIN}$	Differential Input Sensitivity	–	0.2	–	–	V
$V_{DIFFCM}$	Differential Common Mode Range	–	0.8	–	2.5	V
$V_{IL}$	Low Level Input Voltage	–	–	–	0.8	V
$V_{IH}$	High Level Input Voltage	–	2.0	–	–	V
$V_{OH}$	Output High Voltage	15k $\Omega$ to VSS	2.8	–	3.6	V
$V_{OL}$	Output Low Voltage	1.5k $\Omega$ to 3.6V	–	–	0.3	V
$Z_{DRV}$	Driver Output Impedance	External $R_s = 27\Omega$	28	–	44	$\Omega$
$Z_{INP}$	Input Impedance	Exclude pull-up/down	10	–	–	M $\Omega$
$V_{TERM}$	Termination Voltage for Upstream Port Pull-up	–	3.0	–	3.6	V
$V_{CRS}$	Output Signal Crossover Voltage	–	1.3	–	2.0	V
$I_{PD}$	Power Down Current	@SUSPEND, OEN='H'	–	–	10	$\mu\text{A}$

## 5. Package Information

### 5.1 64-LQFP-1010 Package Information

64-LQFP is a 64-pin, 10 x 10 mm Quad Flat Package.

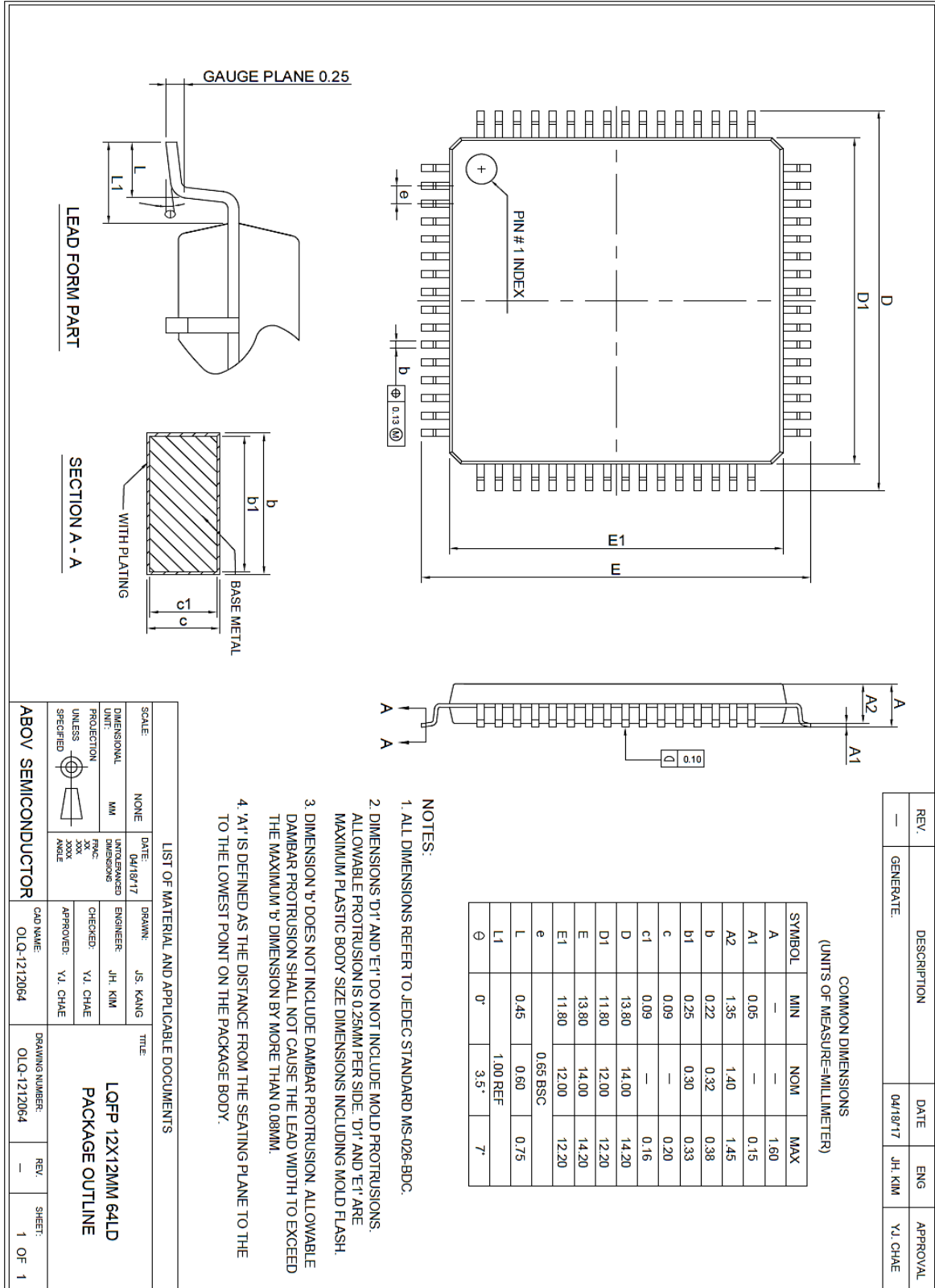
Figure 24. 64-LQFP-1010 Package Dimension



### 5.2 64-LQFP-1212 Package Information

64-LQFP is a 64-pin, 12 x 12 mm Quad Flat Package.

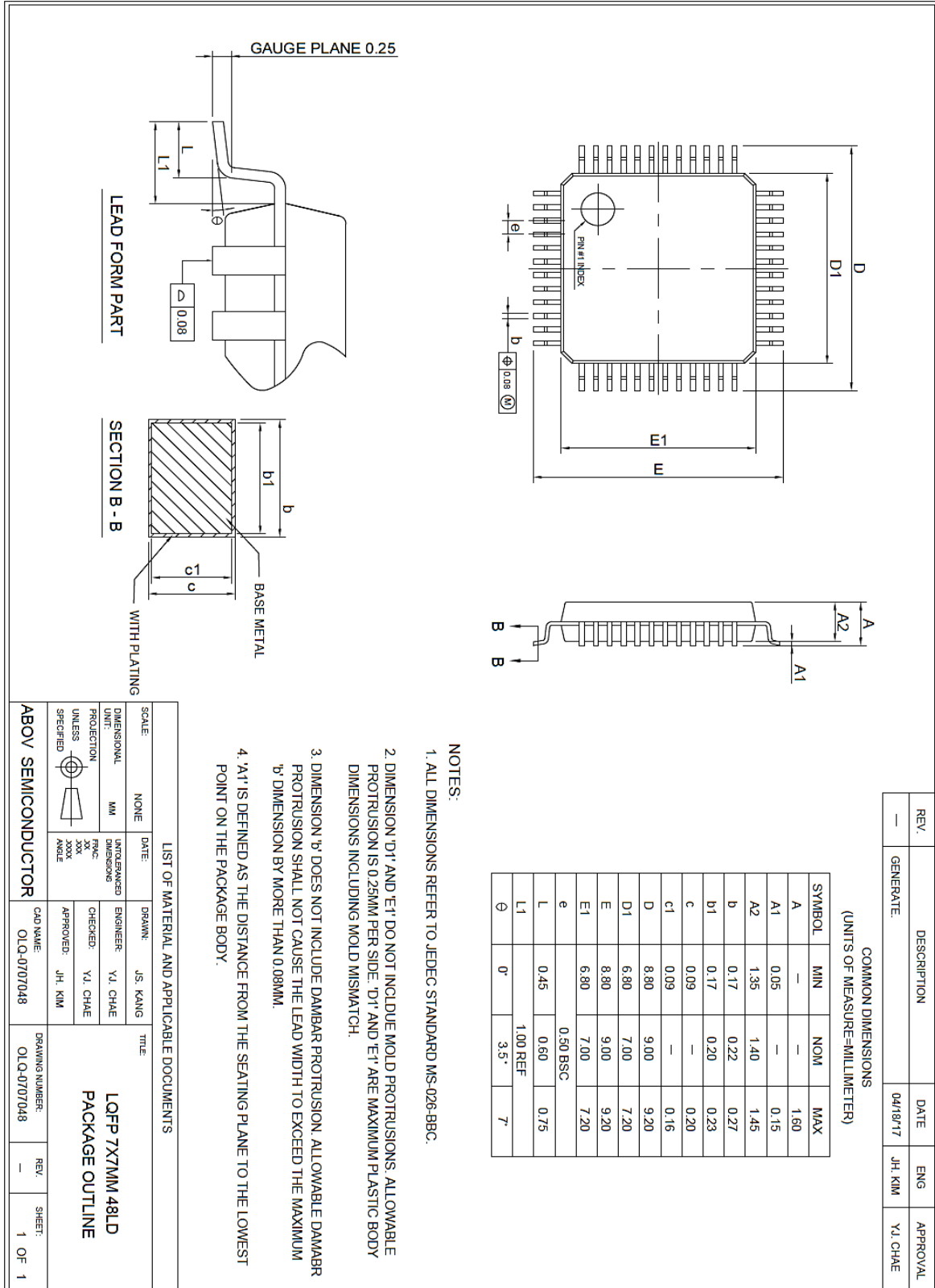
Figure 25. 64-LQFP-1212 Package Dimension



### 5.3 48-LQFP-0707 Package Information

48-LQFP is a 48-pin, 7 x 7 mm Quad Flat Package.

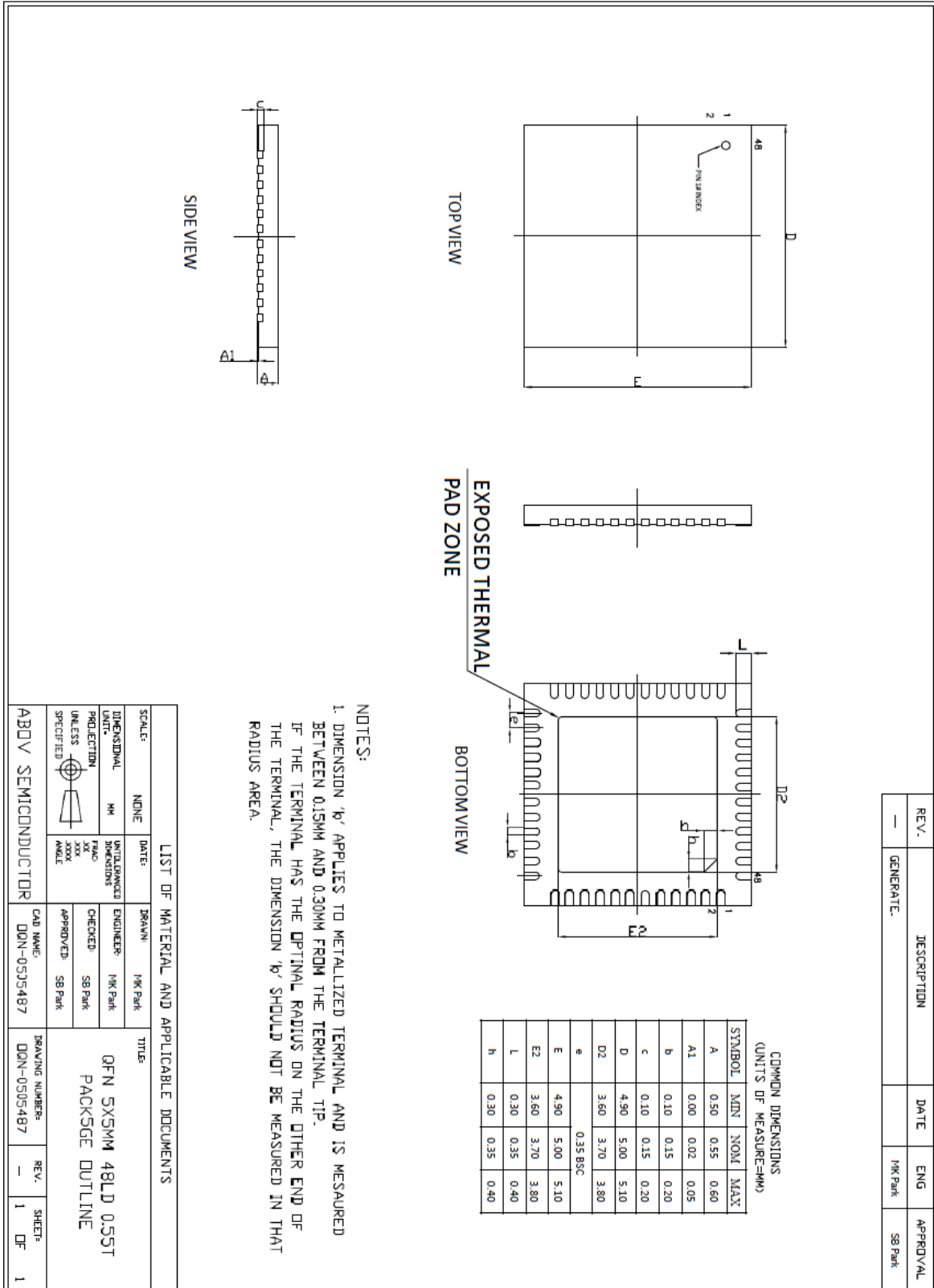
Figure 26. 48-LQFP-0707 Package Dimension



### 5.4 48-QFN-0505 Package Information

48-QFN is a 48-pin, 5 x 5 mm Quad Flat No-lead package.

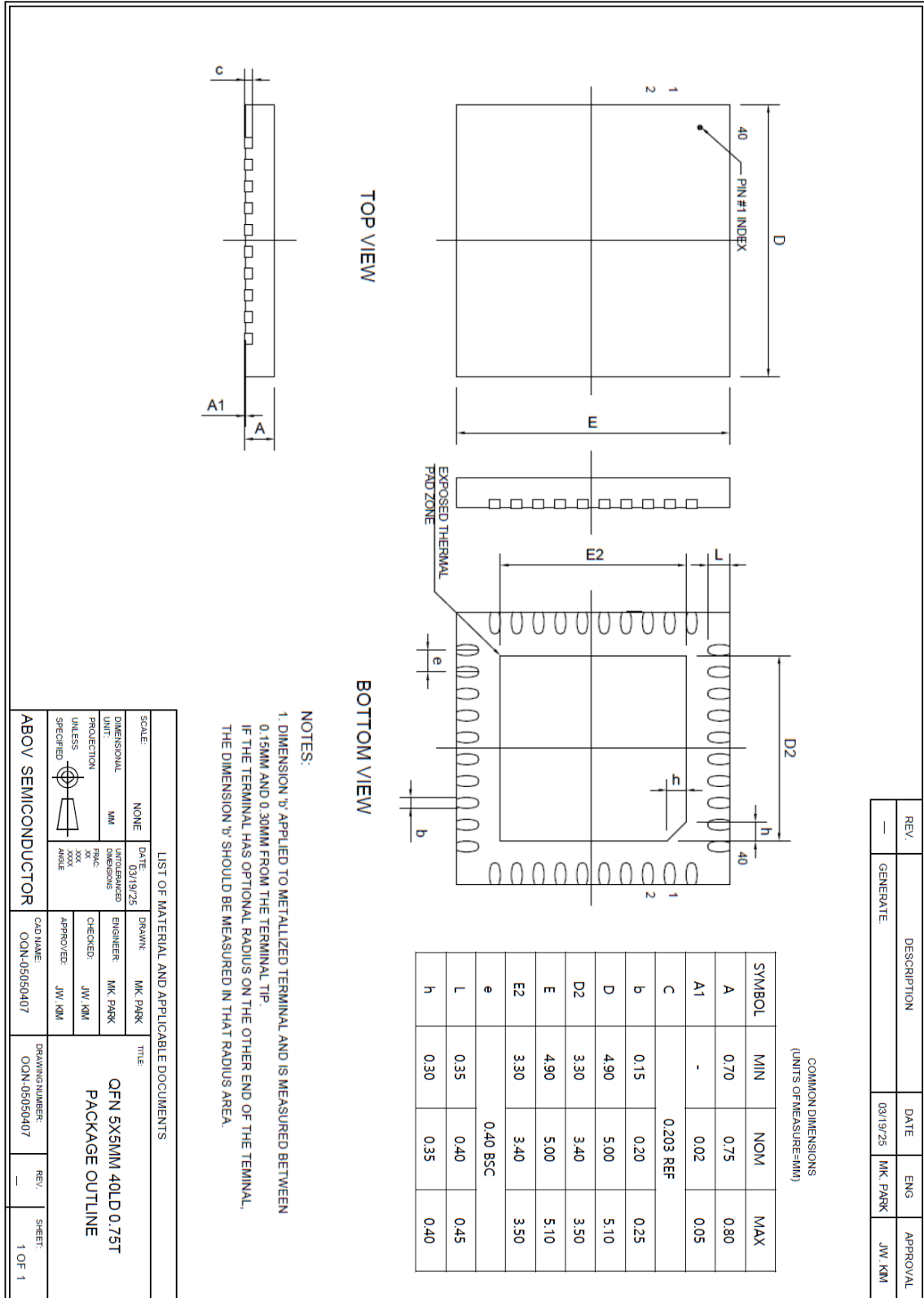
Figure 27. 48-QFN-0505 Package Dimension



### 5.5 40-QFN-0505 Package Information

40-QFN is a 40-pin, 5 x 5 mm Quad Flat No-lead package.

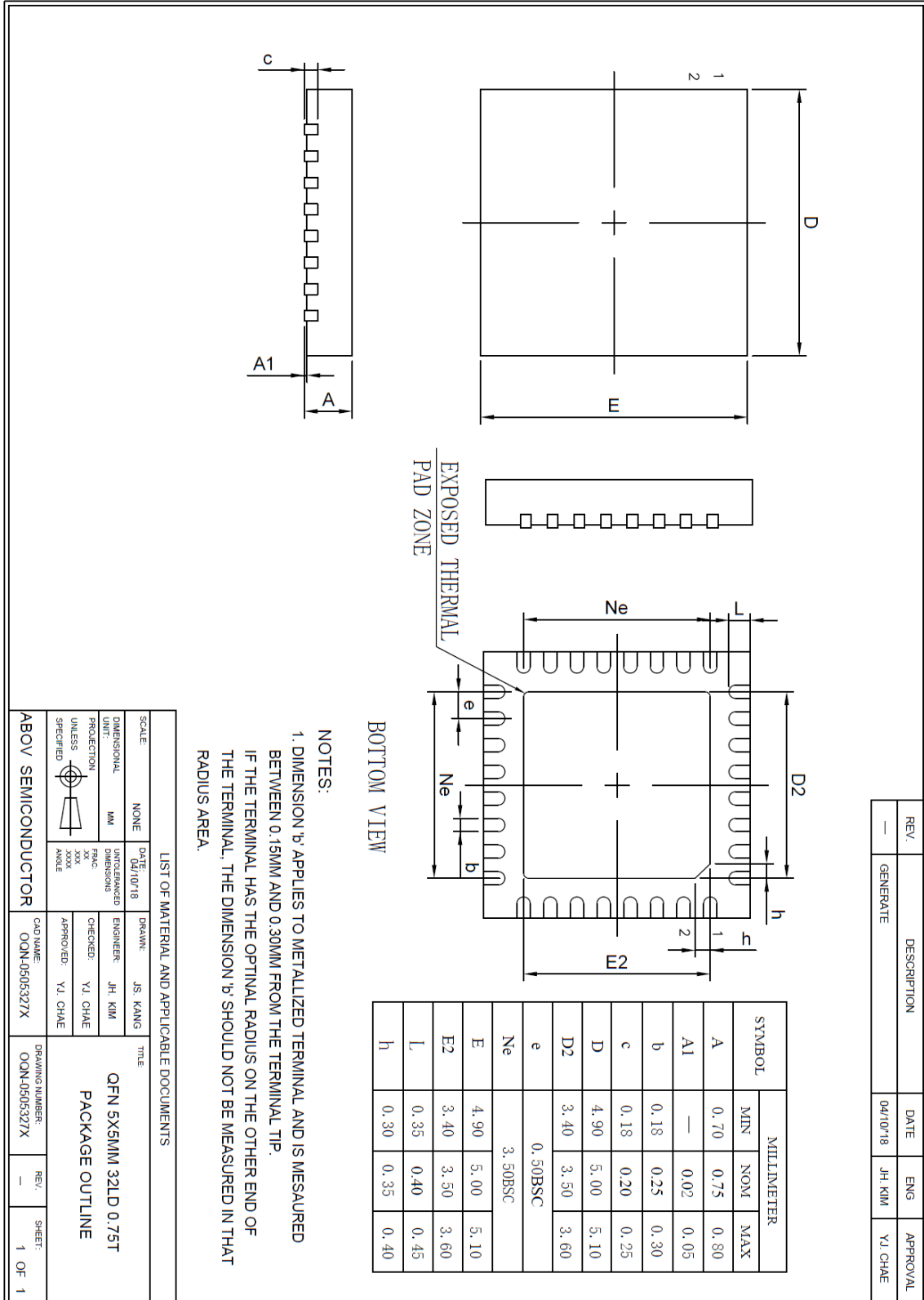
Figure 28. 40-QFN-0505 Package Dimension



### 5.6 32-QFN-0505 Package Information

32-QFN is a 32-pin, 5 x 5 mm Quad Flat No-lead package.

Figure 29. 32-QFN-0505 Package Dimension



## 6. Ordering Information

Figure 30. Device Nomenclature - Part Number Decoder

A31G33		6	R	L	N	(T)
<b>Device family name</b>						
A31G33 = ARM Cortex-M0+ based microcontroller						
<b>Code memory size</b>						
6	256 Kbytes					
<b>Pin count</b>						
R	64 pins					
C	48 pins					
I	40 pins					
K	32 pins					
<b>Package type</b>						
L	LQFP (0.5 mm pin pitch)					
M	LQFP (0.65 mm pin pitch)					
U	QFN					
<b>Temperature</b>						
None	-40 to 85°C (commercial grade)					
<b>Bonding wire</b>						
None	Au wire					
N	Pd-Cu wire					
<b>Packing</b>						
(T)	Tape & reel					
(W)	Wafer					
(C)	Chip carrier					

**NOTE:**

1. For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest [ABOV sales office](#)

## Glossary

This section gives a brief definition of acronyms, abbreviations and terminology used in this document:

- AHB: Advanced High-performance Bus
- APB: Advanced Peripheral Bus
- Byte: Data of 8-bit length
- CRC: Cyclic Redundancy Check
- DMA: Direct Memory Access
- I2C: Inter-Integrated Circuit
- LSB: Least Significant Bit
- LQFP: Low-profile Quad Flat Package
- LVI: Low-Voltage Indicator
- LVR: Low-Voltage Reset
- PGM: Programming
- POR: Power-On Reset
- QFN: Quad Flat No-Lead
- SCU: System Control Unit
- SPI: Serial Peripheral Interface
- UART: Universal Asynchronous Receiver Transmitter
- USART: Universal Synchronous and Asynchronous Receiver Transmitter
- WDT: Watchdog Timer
- Word: Data of 32-bit length

## Revision History

Revision	Date	Notes
1.00	Jan. 06, 2025	Initial release

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