
**CMOS Single-chip 8-bit Microcontroller, Flash Memory 16 KB,
SRAM 768 Bytes, 12-bit ADC**

DS Rev. 1.10

Features**Core and Memory**

- 8-bit M8051 core (8051 Compatible, 2 clocks per cycle)
- 16 KB On-chip Flash (ISP)
- 256 bytes IRAM, 512 bytes XRAM

General Purpose I/O (GPIO)

- Normal I/O: 30 Port

Timer/Counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- Watchdog Timer (WDT) 8-bit × 1-ch
- 8-bit × 1-ch (T0)
- 16-bit × 2-ch (T1/T2)

Programmable Pulse Generation

- Pulse generation (by T1/T2)
- 8-bit PWM (by T0)

Buzzer

- 8-bit × 1-ch

Watch Timer (WT)

- 3.91 ms / 0.25 s / 0.5 s / 1 s / 1-minute intervals at 32.768 kHz

12-bit A/D Converter

- 15 Input channels
- Power down wake-up function

16-bit CRC/Checksum Generator

- Auto and User CRC/Checksum mode

8bit I2C x 1 Channel**8bit SPI x 1 Channel****8bit UART x 2 Channels****128-Bit Unique ID****Power-on Reset**

- Reset release level (1.4 V)

Low Voltage Reset

- 14 Level detect (1.60 V, 2.00 V, ..., 4.40 V)

Low Voltage Indicator

- 13 Level detect (2.00 V, 2.10 V, ..., 4.40 V)

Interrupt Sources

- External Interrupts (EINT0~4/5/6/7~A/10/11/12) (7)
- Timer 0/1/2 (4), WDT (1), BIT (1), WT (1)
- UART0/1 (4), I2C/SPI (1/1), ADC (1), ADC Wake-up (1)

Internal High Frequency RC Oscillator

- 16 MHz ±1.0% (TA=-20 ~ +70°C, User trim)

Power-down Mode

- STOP, IDLE mode

Operating Voltage and Frequency

- 2.0 V to 5.5 V (@32 to 38 kHz with SX-tal)
- 2.2 V to 5.5 V (@0.4 to 4.2 MHz with X-tal)
- 2.4 V to 5.5 V (@0.4 to 8 MHz with X-tal)
- 2.7 V to 5.5 V (@0.4 to 12 MHz with X-tal)
- 1.8 V to 5.5 V (@0.5 to 16 MHz with IRC)
- Voltage dropout converter included for core

Operating Temperature

- -40°C ~ +105°C

Package Type

- 32-LQFP
- 32-QFN
- 28-SOP
- 24-QFN
- 20-SOP
- 20-TSSOP
- Pb-free package

Product Selection Table**Table 1. Device Summary**

Part Number	Flash	IRAM/XRAM	UART	I2C	SPI	Timer	ADC	I/O	Package
MC96F8316PL	16KB	256/512B	2	1	1	3	15 ch	30	32-LQFP
MC96F8316PU	16KB	256/512B	2	1	1	3	15 ch	30	32-QFN-0505
MC96F8316PM	16KB	256/512B	2	1	1	3	12 ch	26	28-SOP
MC96F8216PU	16KB	256/512B	2	1	1	3	11 ch	22	24-QFN-0404
MC96F8216PD	16KB	256/512B	2	1	0	3	8 ch	18	20-SOP
MC96F8216PR	16KB	256/512B	2	1	0	3	8 ch	18	20-TSSOP

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1. Description

The MC96F8316P is an advanced CMOS 8-bit microcontroller with 16 Kbytes of flash memory. This is a powerful microcontroller which provides a highly flexible and cost-effective solution to many embedded control applications. This provides the following features : 16 Kbytes of flash memory, 256 bytes of IRAM, 512 bytes of XRAM , general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, 8-bit PWM output, watch timer, buzzer driving port, SPI, UART, I2C, 12-bit A/D converter, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F8316P also supports power saving modes to reduce power consumption.

Table 2 describes features of MC96F8316P and peripheral counts.

1.1 Device Overview

Table 2. MC96F8316P Device Features and Peripheral Counts

Peripheral		MC96F8316P
CPU		8-bit CISC core (M8051, 2 clocks per cycle)
Flash		<ul style="list-style-type: none"> • 16 Kbytes with self r/w capability • On-chip debug and ISP • Endurance: <ul style="list-style-type: none"> - 10,000 times (Sector 0~503) - 100,000 times (Sector 504~511)
IRAM		256 bytes
XRAM		512 bytes
GPIO		<ul style="list-style-type: none"> • Normal I/O • 30 ports: P0[6:0], P1[7:0], P2[6:0] , P3[7:0]
Timer/counter		<ul style="list-style-type: none"> • BIT 8-bit x 1-ch • WDT 8-bit x 1-ch: 5kHz internal RC oscillator for WDT • 8-bit x 1-ch (T0) • 16-bit x 2-ch (T1/T2) • Watch Timer (WT)
BUZZER		8-bit x 1-ch
Programmable pulse generation		<ul style="list-style-type: none"> • Pulse generation (by T1/T2) • 8-Bit PWM (by T0)
ADC		<ul style="list-style-type: none"> • 12-bit ADC, 15 input channels • Power down wake-up function
CRC and checksum generator		<ul style="list-style-type: none"> • 16-bit • Auto and user CRC/ checksum mode
Reset	Power-on Reset	Reset release level (1.4 V)
	Low voltage reset	14 Level detect (1.60 V, 2.0 V, ..., 4.4 V)

Table 2. MC96F8316P Device Features and Peripheral Counts (continued)

Peripheral	MC96F8316P
Low voltage indicator	13 Level detect (2.0 V, ..., 4.4 V)
Seral interface	Two UARTs, One I2C, One SPI
Power consumption	Stop and Idle modes
Internal RC oscillator	16 MHz \pm 1.0% ($T_A = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, User trim)
Operating voltage and frequency	<ul style="list-style-type: none"> • 2.0 V to 5.5 V @ 32 to 38 kHz with SX-tal • 2.2 V to 5.5 V @ 0.4 to 4.2 MHz with X-tal • 2.4 V to 5.5 V @ 0.4 to 8.0 MHz with X-tal • 2.7 V to 5.5 V @ 0.4 to 12.0 MHz with X-tal • 1.8 V to 5.5 V @ 0.5 to 16 MHz with IRC • Voltage dropout converter included for core
Minimum instruction execution time	<ul style="list-style-type: none"> • 0.125 μs @ 16MHz IRC • 61 μs at 32.768 kHz sub clock
Operating temperature	-40°C to $+105^{\circ}\text{C}$
Package type	<ul style="list-style-type: none"> • 32-LQFP • 32-QFN 05x05 • 28-SOP • 24-QFN 04x04 • 20-SOP • 20-TSSOP • Pb-free package

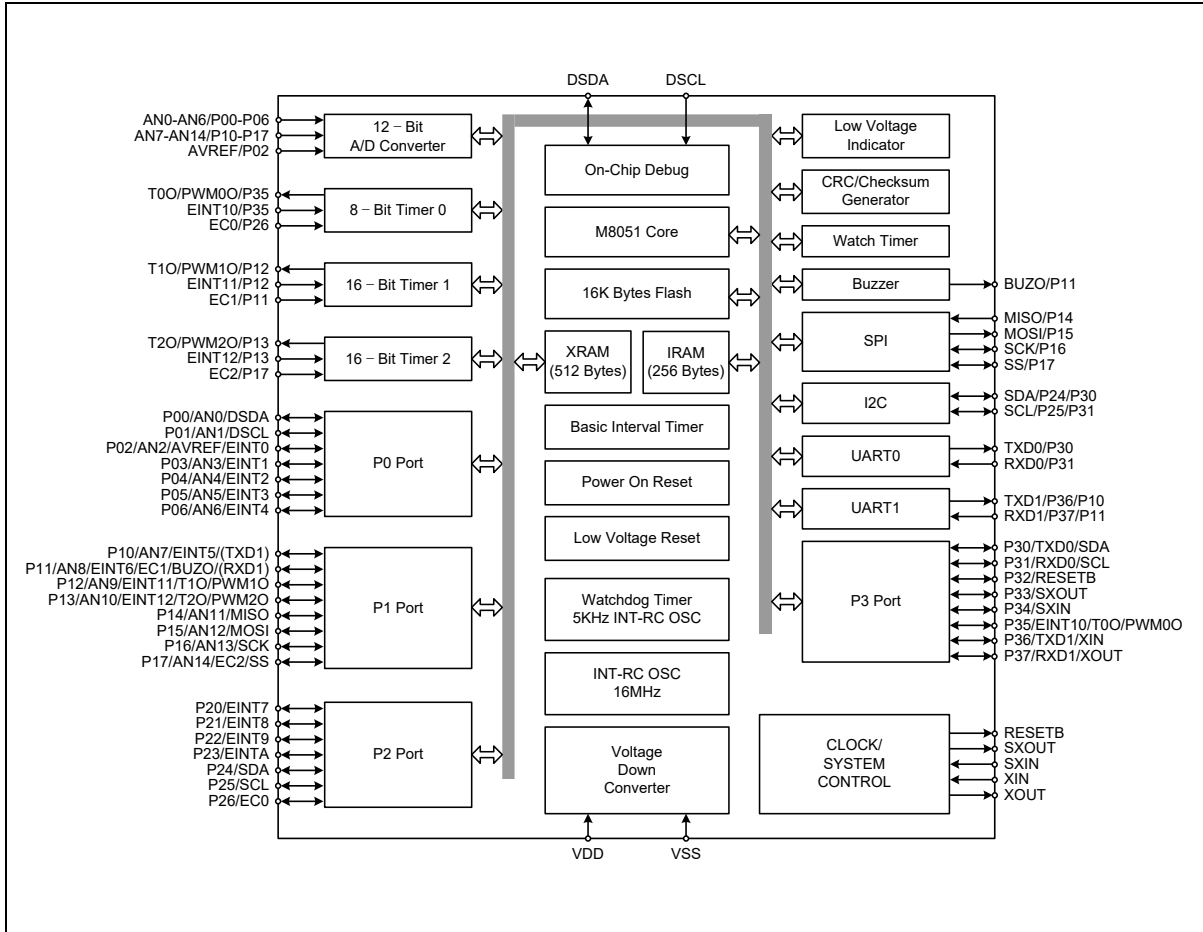
Table 3. Summary of MC96F8316P Peripherals

Peripheral		MC96F8316PL MC96F8316PU	MC96F8316PM	MC96F8216PU	MC96F8216PD MC96F8216PR
Code Flash memory		16 KB	16 KB	16 KB	16 KB
IRAM/XRAM		256/512 bytes	256/512 bytes	256/512 bytes	256/512 bytes
Timers	General purpose	2 (16-bit), 1 (8-bit)			
	WDT	1			
	BIT	1			
Communication interfaces	SPI	1	1	1	0
	I2C	1	1	1	1
	UART	2	2	2	2
WT		1			
BUZZER		1			
GPIO		30	26	22	18
ADCs		50 ksps	50 ksps	50 ksps	50 ksps
Number of channels		15	12	11	8
Max. CPU frequency		16 MHz			
128 Unique ID		1			
CRC/Checksum		1 (16-bit)			
Operating voltage		1.8 V to 5.5 V			
Operating temperature		Ambient operating temperature : -40°C to 105°C			
Packages		32-LQFP 32-QFN	28-SOP	24-QFN	20-SOP 20-TSSOP

1.2 MC96F8316P Block Diagram

Figure 1 describes MC96F8316P in a block diagram.

Figure 1. MC96F8316P Block Diagram



2. Pinouts and Pin Descriptions

In this chapter, MC96F8316P pinouts and pin descriptions are described.

2.1 Pinouts

Figure 2. MC96F8316PL 32-LQFP Pinouts

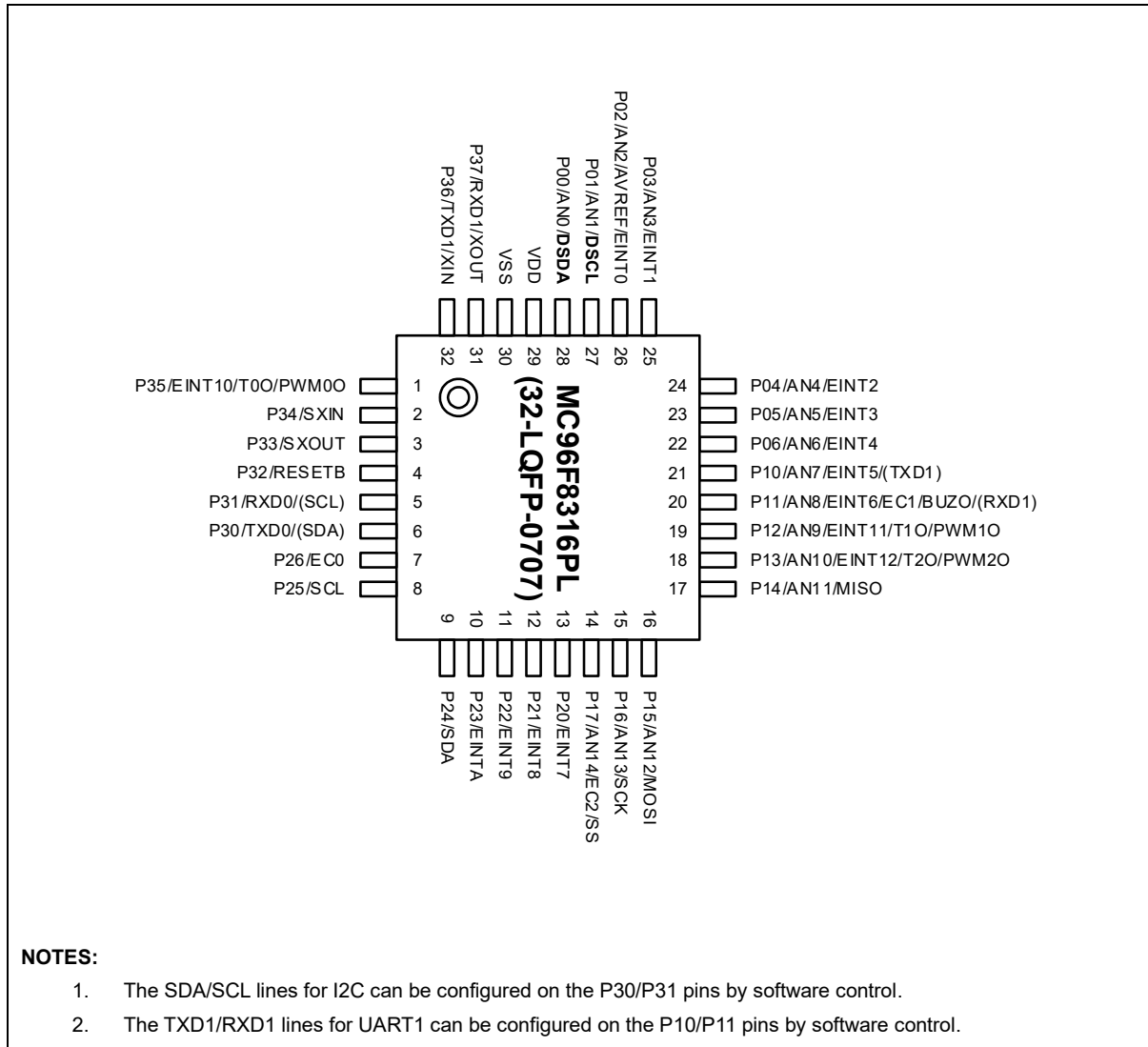


Figure 3. MC96F8316PU 32-QFN Pinouts

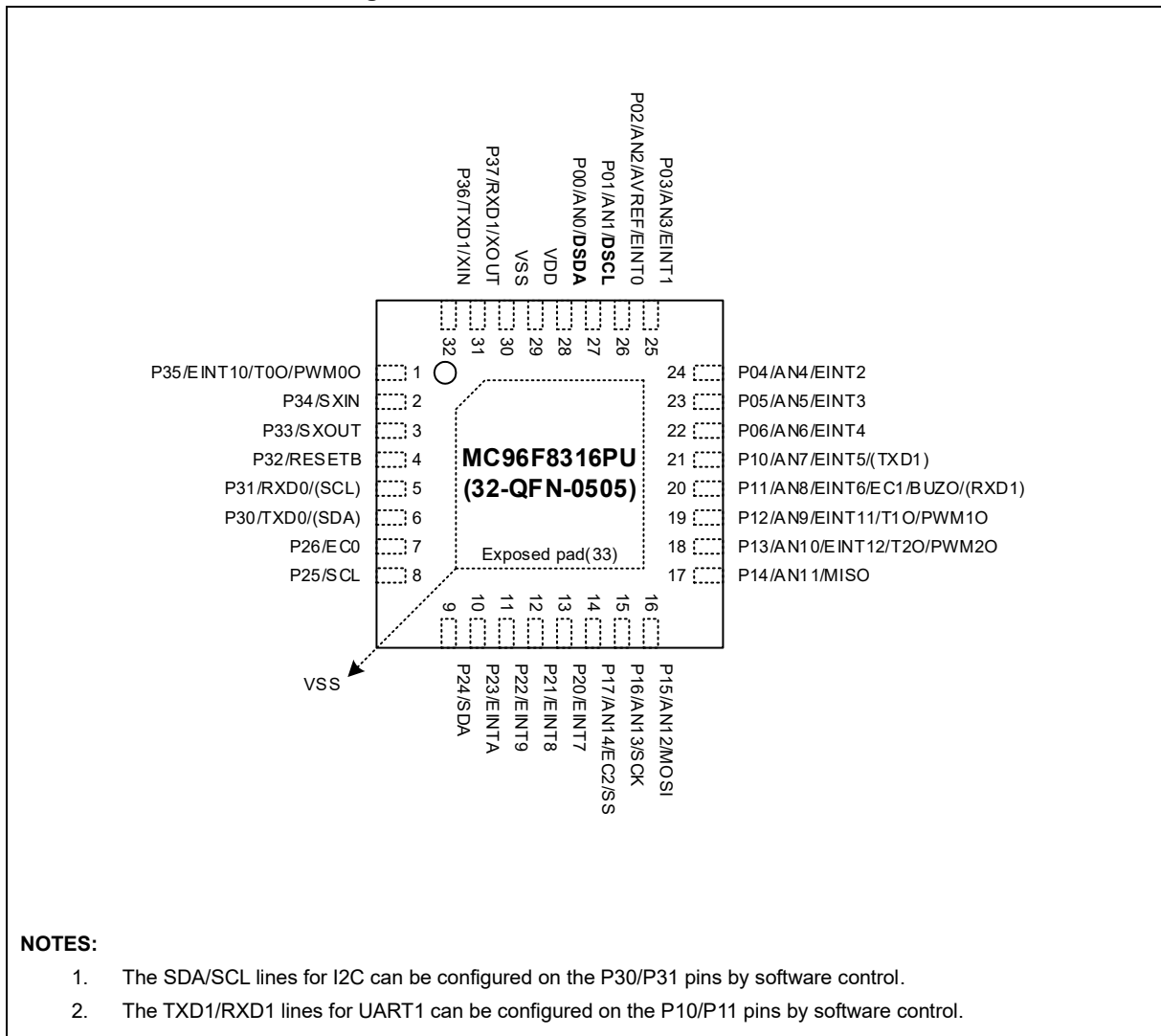


Figure 4. MC96F8316PM 28-SOP Pinouts

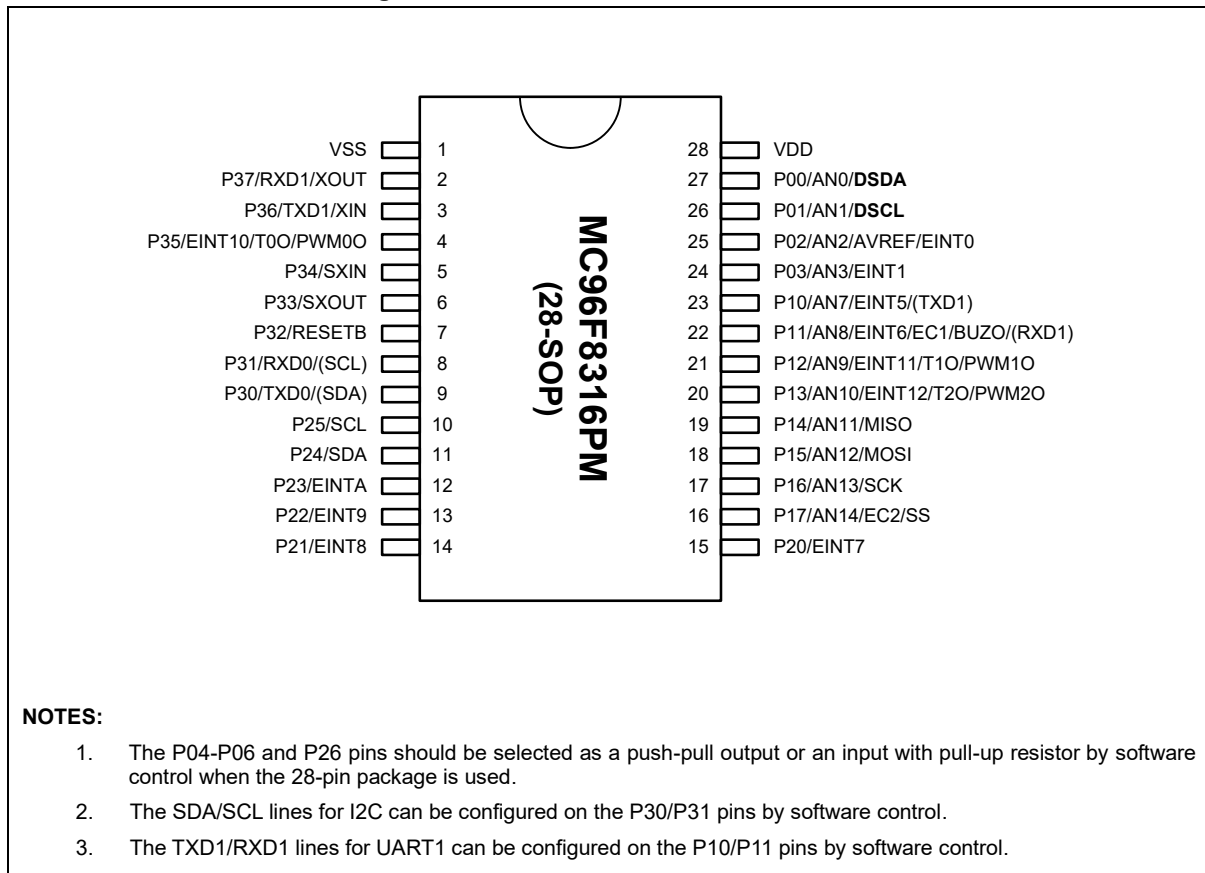


Figure 5. MC96F8216PU 24-QFN Pinouts

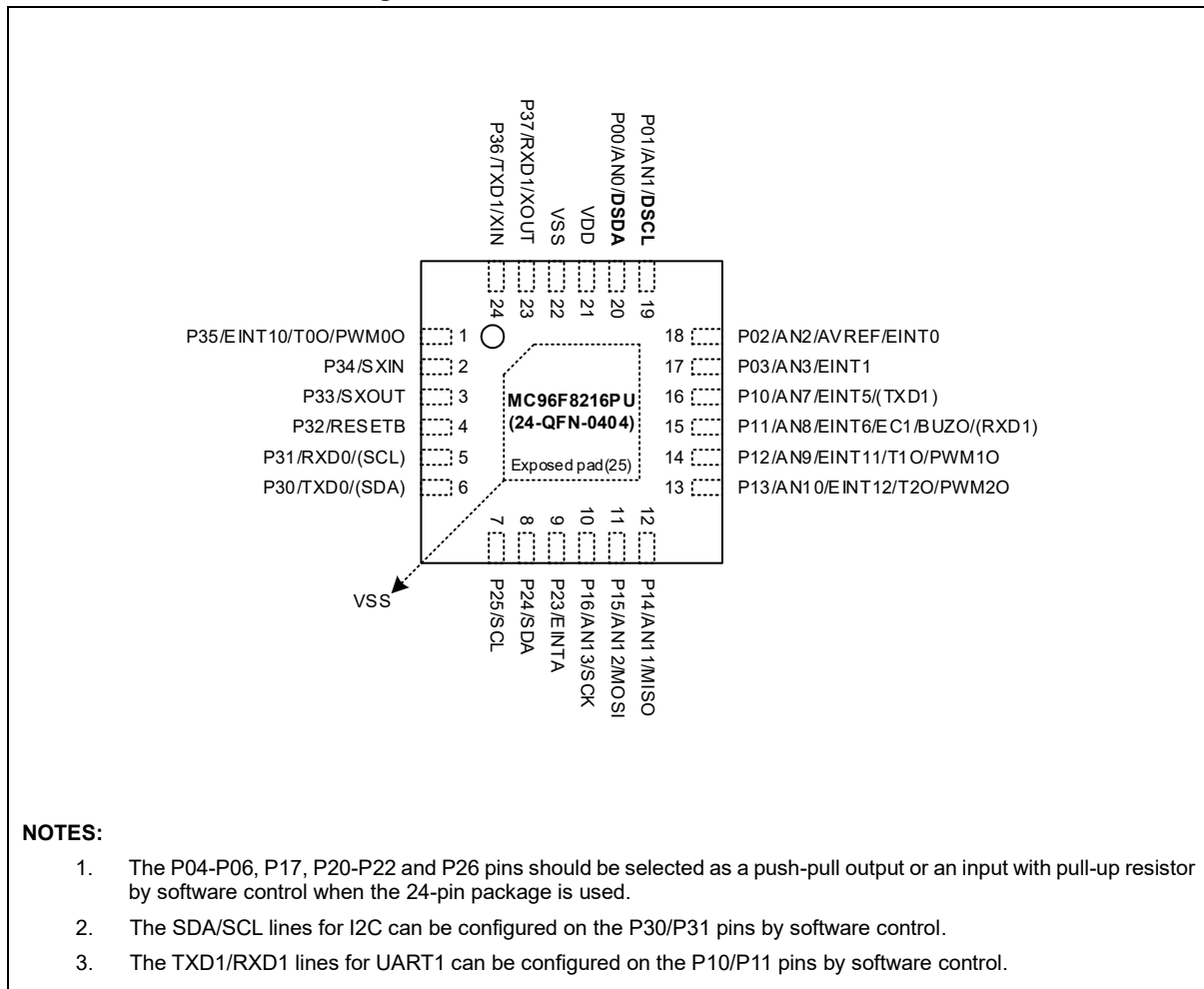


Figure 6. MC96F8216PD 20-SOP Pinouts

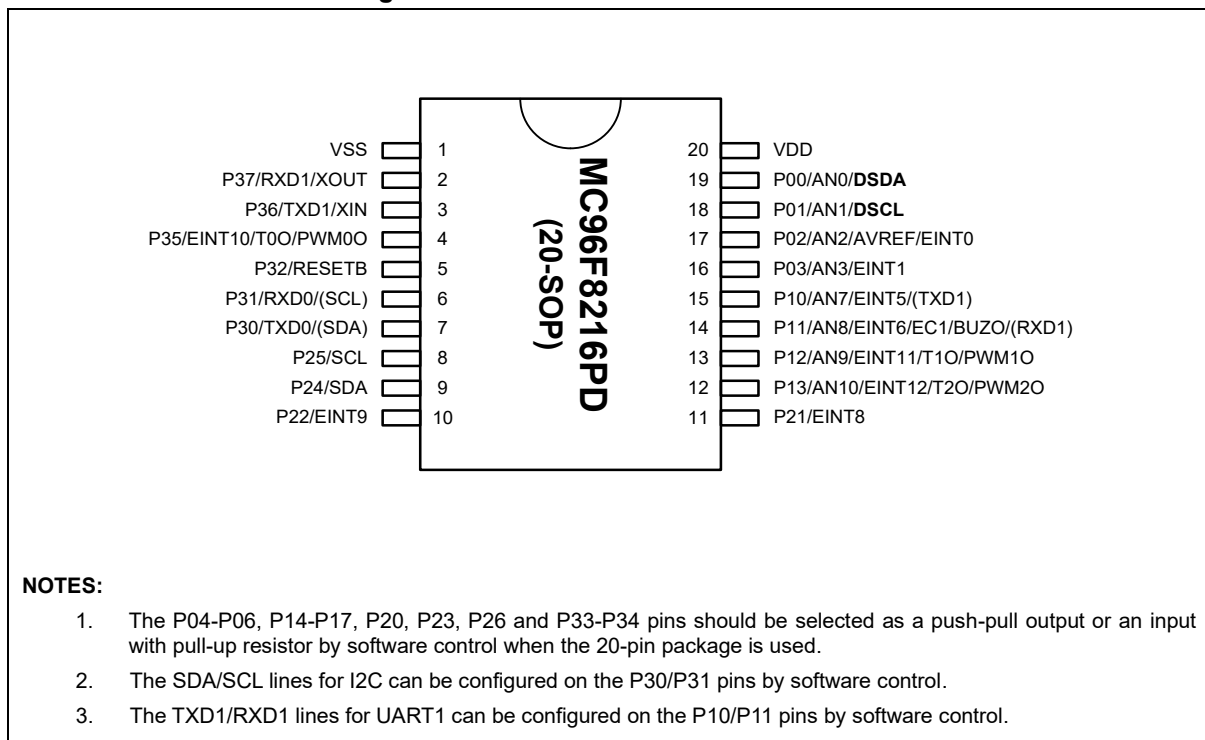
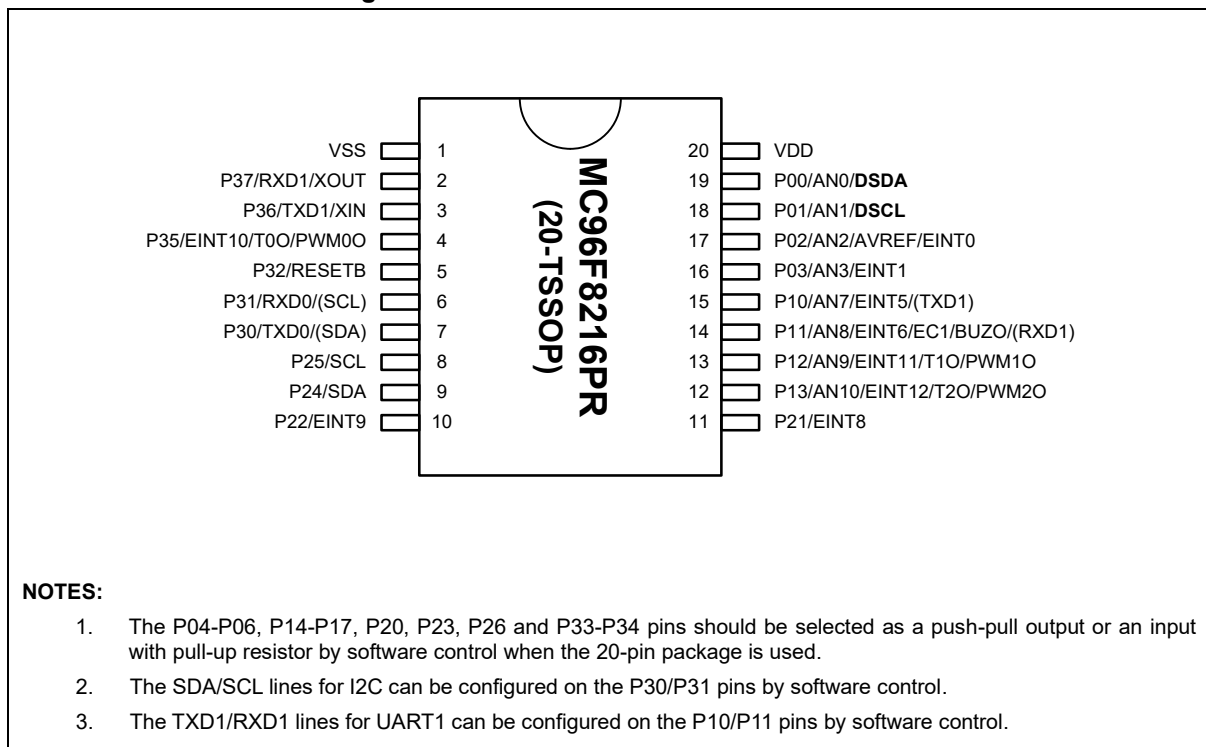


Figure 7. MC96F8216PR 20-TSSOP Pinouts



2.2 Pin Description

Table 4. Pin Description

Pin Name	I/O	Function	@reset	Shared With
P00	I/O	The port 0 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P04 – P06 are only in the 32-Pin package	Input	AN0/DSDA
P01				AN1/DSCL
P02				AN2/AVREF/EINT0
P03				AN3/EINT1
P04				AN4/EINT2
P05				AN5/EINT3
P06				AN6/EINT4
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P17 is not in the 24-Pin package. The P14 – P17 are not in the 20-Pin package.	Input	AN7/EINT5/TXD1
P11				AN8/EINT6/EC1/BUZO/RXD1
P12				AN9/EINT11/T10/PWM1O
P13				AN10/EINT12/T20/PWM2O
P14				AN11/MISO
P15				AN12/MOSI
P16				AN13/SCK
P17				AN14/EC2/SS
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P20 – P22 are not in the 24-Pin package. The P20 and P23 are not in the 20-Pin package. The P26 is only in the 32-Pin package.	Input	EINT7
P21				EINT8
P22				EINT9
P23				EINTA
P24				SDA
P25				SCL
P26				EC0
P30	I/O	Port 3 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P33 – P34 are not in the 20-Pin package.	Input	TXD0/SDA
P31				RXD0/SCL
P32				RESETB
P33				SXOUT
P34				SXIN
P35				EINT10/T00/PWM0O
P36				TXD1/XIN
P37				RXD1/XOUT

Table 4. Pin Description (continued)

Pin Name	I/O	Function	@reset	Shared With
EINT0	I/O	External interrupt inputs	Input	P02/AN2/AVREF
EINT1				P03/AN3
EINT2				P04/AN4
EINT3				P05/AN5
EINT4				P06/AN6
EINT5				P10/AN7/TXD1
EINT6				P11/AN8/EC1/BUZO/RXD1
EINT7				P20
EINT8				P21
EINT9				P22
EINTA				P23
EINT10				I/O
EINT11	I/O	External interrupt and Timer 1 capture input	Input	P12/AN9/T10/PWM10
EINT12	I/O	External interrupt and Timer 2 capture input	Input	P13/AN10/T20/PWM20
T00	I/O	Timer 0 interval output	Input	P35/EINT10/PWM00
T10	I/O	Timer 1 interval output	Input	P12/AN9/EINT11/PWM10
T20	I/O	Timer 2 interval output	Input	P13/AN10/EINT12/PWM20
PWM00	I/O	Timer 0 PWM output	Input	P35/EINT10/T00
PWM10	I/O	Timer 1 pulse output	Input	P12/AN9/EINT11/T10
PWM20	I/O	Timer 2 pulse output	Input	P13/AN10/EINT12/T20
EC0	I/O	Timer 0 event count input	Input	P26
EC1	I/O	Timer 1 event count input	Input	P11/AN8/EINT6/BUZO/RXD1
EC2	I/O	Timer 2 event count input	Input	P17/AN14/SS
BUZO	I/O	Buzzer signal output	Input	P11/AN8/EINT6/EC1/RXD1
SCK	I/O	Serial clock input/output	Input	P16/AN13
MISO	I/O	Serial data input/output	Input	P14/AN11
MOSI	I/O	Serial data input/output	Input	P15/AN12
SS	I/O	Slave select input	Input	P17/AN14/EC2
TXD0	I/O	UART data output	Input	P30
RXD0	I/O	UART data input	Input	P31
TXD1	I/O	UART data output	Input	P36/XIN P10/AN7/EINT5
RXD1	I/O	UART data input	Input	P37/XOUT P11/AN8/EINT6/EC1/BUZO

Table 4. Pin Description (continued)

Pin Name	I/O	Function	@reset	Shared With
SCL	I/O	I2C clock input/output	Input	P31/RXD0 P25
SDA	I/O	I2C data input/output	Input	P30/TXD0 P24
AVREF	I/O	A/D converter reference voltage	Input	P02/AN2/EINT0
AN0	I/O	A/D converter analog input channels	Input	P00/DSDA
AN1				P01/DSCL
AN2				P02/AVREF/EINT0
AN3				P03/EINT1
AN4				P04/EINT2
AN5				P05/EINT3
AN6				P06/EINT4
AN7				P10/EINT5/TXD1
AN8				P11/EINT6/EC1/BUZO/RXD1
AN9				P12/EINT11/T10/PWM1O
AN10				P13/EINT12/T2O/PWM2O
AN11				P14/MISO
AN12				P15/MOSI
AN13				P16/SCK
AN14				P17/EC2/SS
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by "CONFIGURE OPTION"	Input	P32
DSDA	I/O	On-chip debugger data input/output	Input	P00
DSCL	I/O	On-chip debugger clock input	Input	P01
XIN	I/O	Main oscillator pins	Input	P36/TXD1
XOUT				P37/RXD1
SXIN	I/O	Sub oscillator pins	Input	P34
SXOUT				P33
VDD, VSS	–	Power input pins	–	–

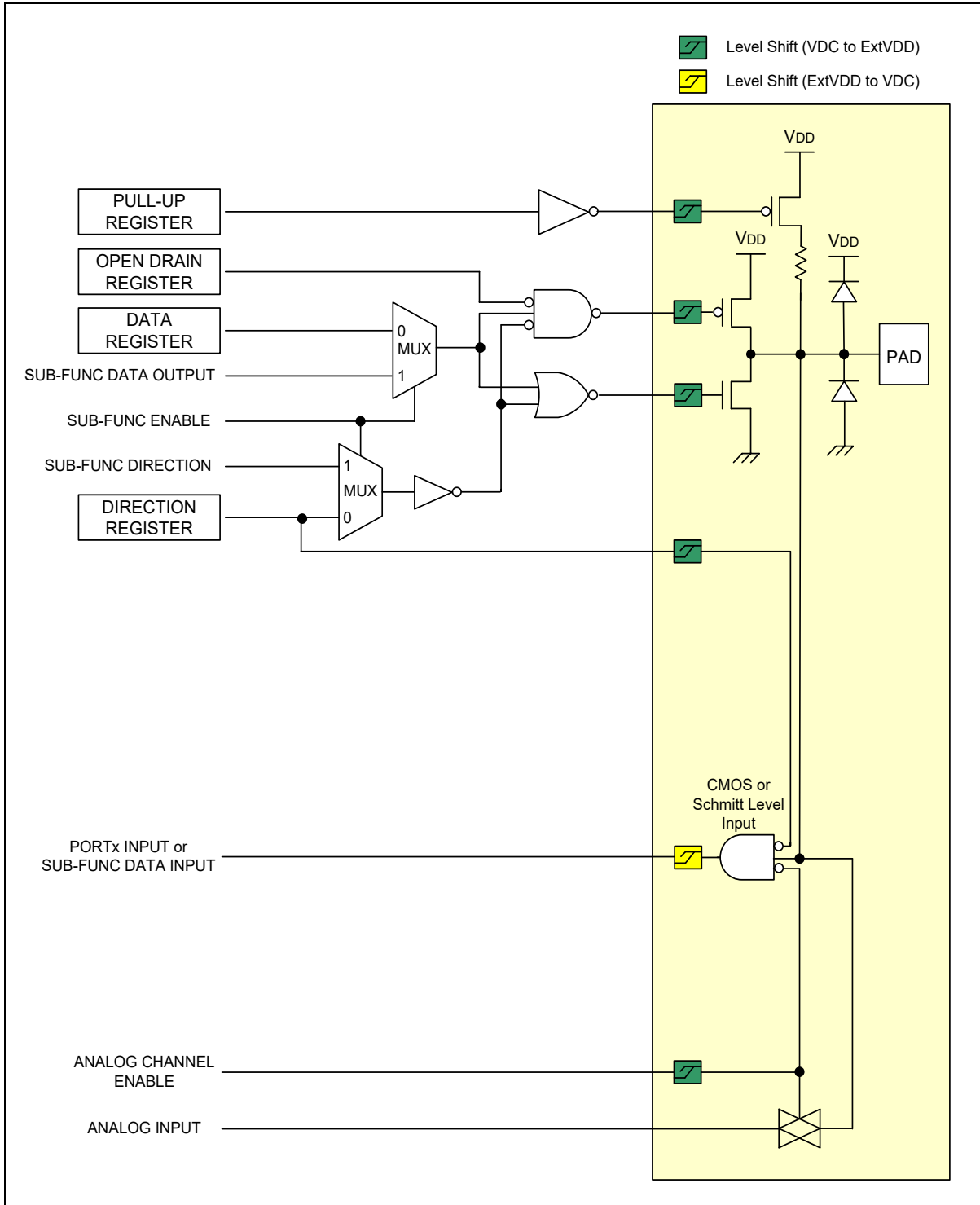
NOTES:

1. The P04-P06 and P26 are not in the 28-Pin package.
2. The P04-P06, P17, P20-P22, and P26 are not in the 24-Pin package.
3. The P04-P06, P14-P17, P20, P23, P26 and P33-P34 are not in the 20-Pin package.
4. The P32/RESETB pin is configured as one of the P32 and the RESETB pin by the "CONFIGURE OPTION".
5. If the P00/DSDA and P01/DSCL pins are connected to an emulator during Power-on Reset, the pins are automatically configured as the debugger pins.
6. The P00/DSDA and P01/DSCL pins are configured as inputs with internal pull-up resistor only during the reset or Power-on Reset.
7. The P37/XOUT, P36/XIN, P34/SXIN, and P33/SXOUT pins are configured as a function pin by software control.

3. Port Structures

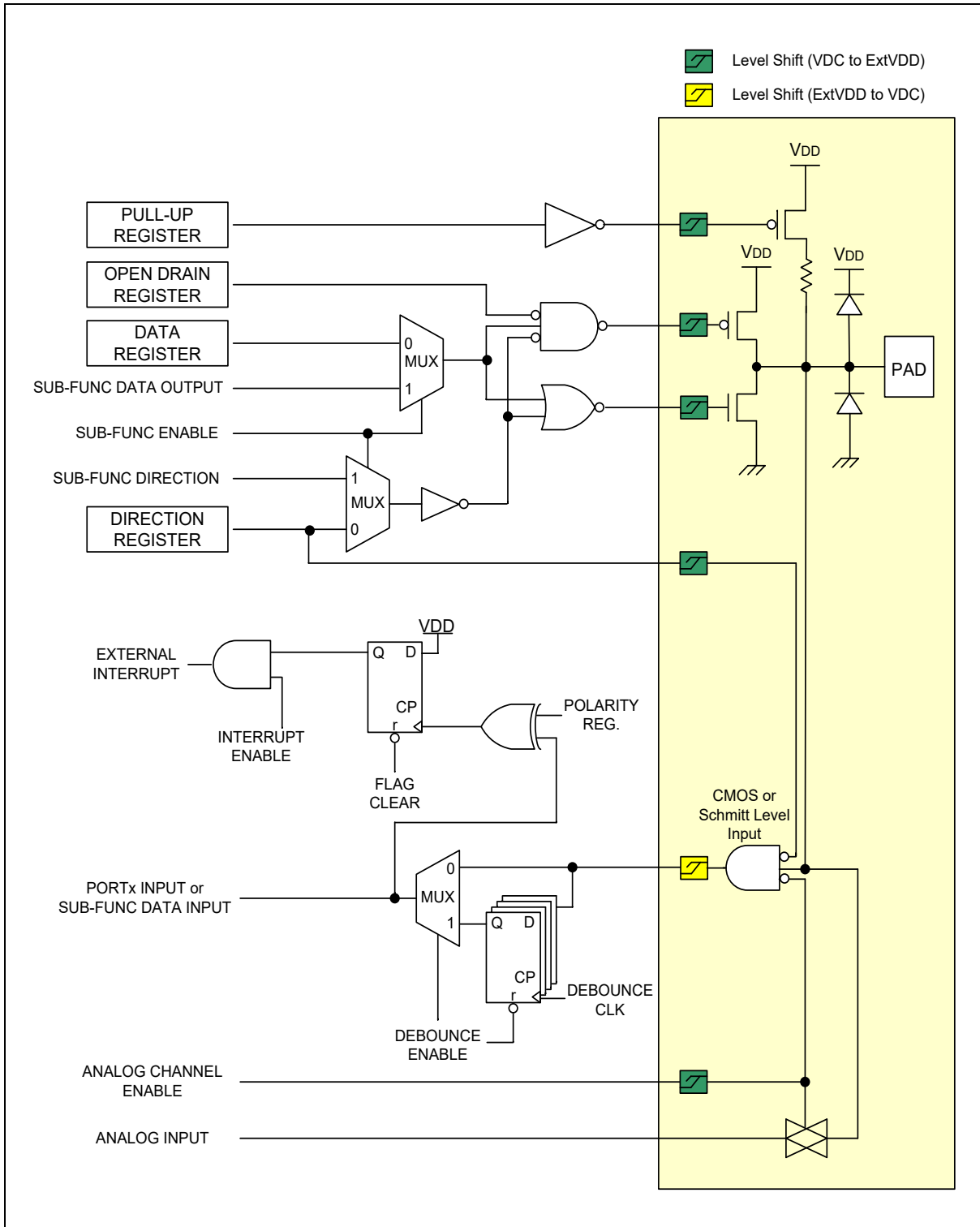
3.1 GPIO Port Structure

Figure 8. General Purpose I/O Port Structure



3.2 External Interrupt I/O Port Structure

Figure 9. External Interrupt I/O Port Structure



4. Memory Organization

MC96F8316P addresses four separate memory spaces:

- Program memory
- Flash user memory
- Data memory
- XRAM memory

By means of this logical separation of the memory, an 8-bit CPU address can access the data memory more rapidly. 16-bit data memory address is generated through the DPTR register.

MC96F8316P provides on-chip 16 Kbytes of ISP type Flash program memory, which is readable and writable. Internal data memory (IRAM) is 256 bytes, and it includes the stack area. External data memory (XRAM) is 512 bytes.

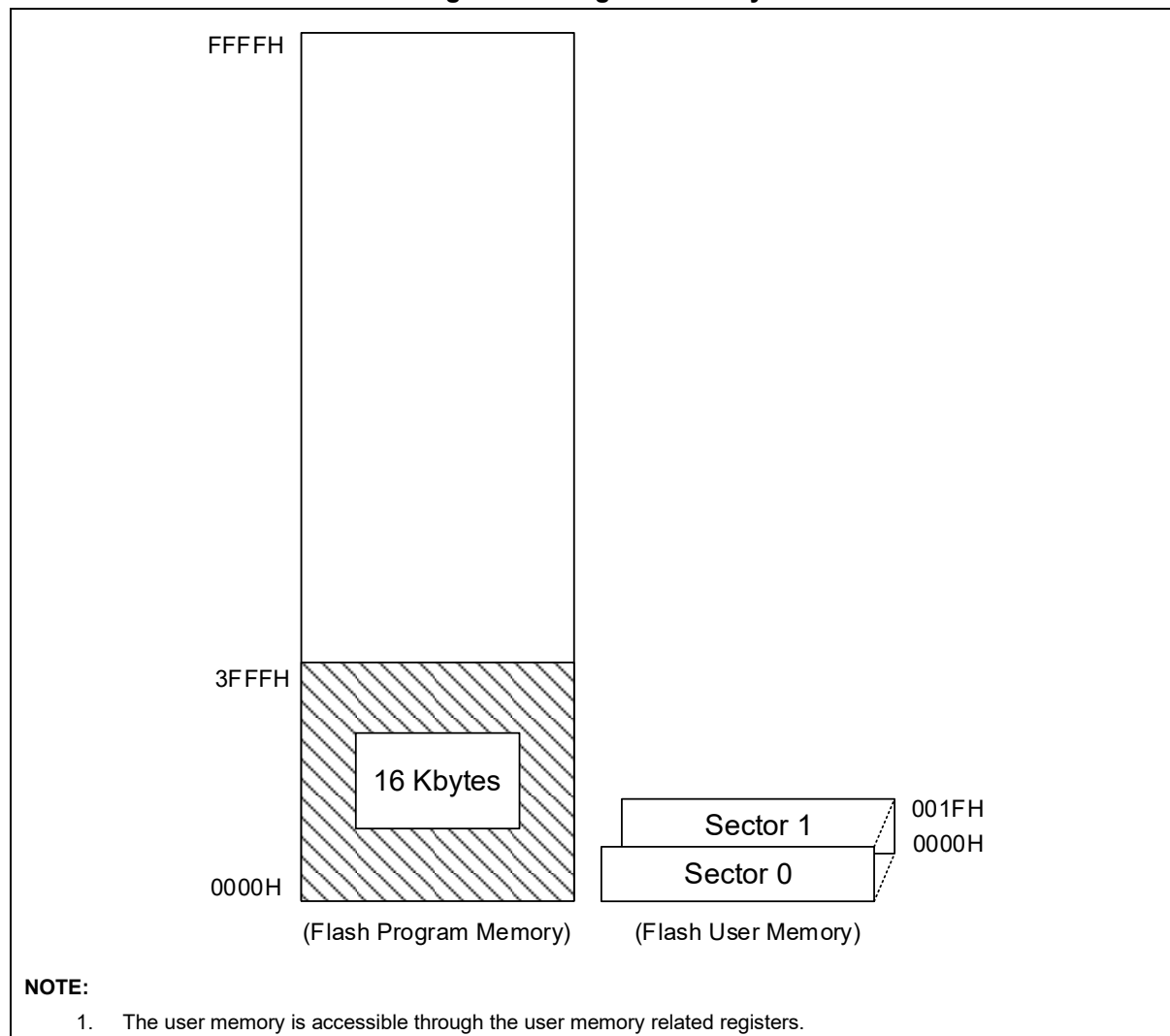
4.1 Program Memory

A 16-bit program counter can address up to 64 Kbytes, but MC96F8316P has only 16 Kbytes program memory space. After reset, CPU begins execution from location 0000H. Each interrupt is assigned to a fixed location of the program memory. The interrupt causes the CPU to jump to that location, where it commences an execution of a service routine.

For example, an external interrupt 1 is assigned to location 002BH. If the external interrupt 1 is going to be used, its service routine must begin at location 002BH. If the interrupt is not going to be used, its service location is available as general-purpose program memory. If an interrupt service routine is short enough (frequent cases with a control application), the service routine can reside entirely within an 8 bytes interval.

A longer service routine can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use. Figure 10 shows a map of the lower part of the program memory.

Figure 10. Program Memory



More detailed description of program memory is described in [Chapter 22. Flash Memory](#).

4.2 Flash User Memory

Flash user memory has a 64 bytes memory space. This memory is accessible through the user memory related registers.

4.3 Internal Data Memory

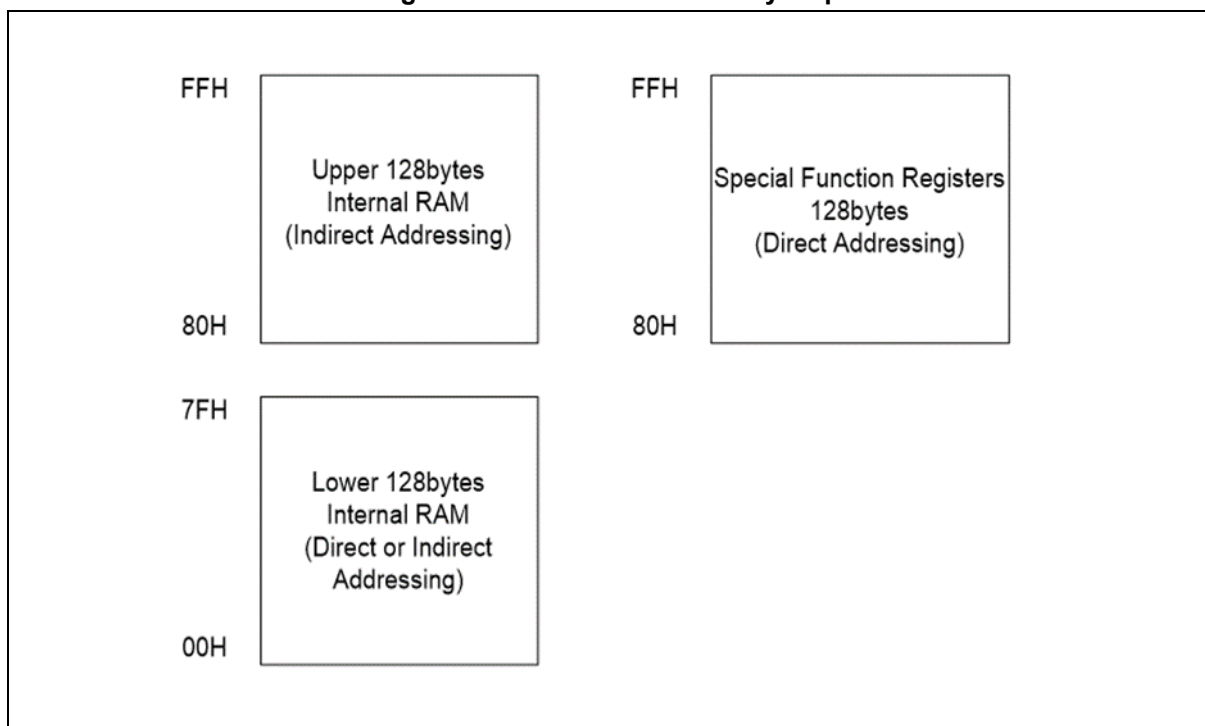
Internal data memory is divided into three spaces as shown in Figure 11. Those three spaces are generally called as,

- Lower 128 bytes
- Upper 128 bytes
- Special Function Registers (SFR space)

Internal data memory addresses are always one byte wide, which implies an address space of 256 bytes.

In fact, the addressing modes of the internal data memory can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. By means of this method, the upper 128 bytes and SFR space can occupy the same block of addresses, 80H through FFH, although they are physically separate entities as shown in Figure 11.

Figure 11. Internal Data Memory Map

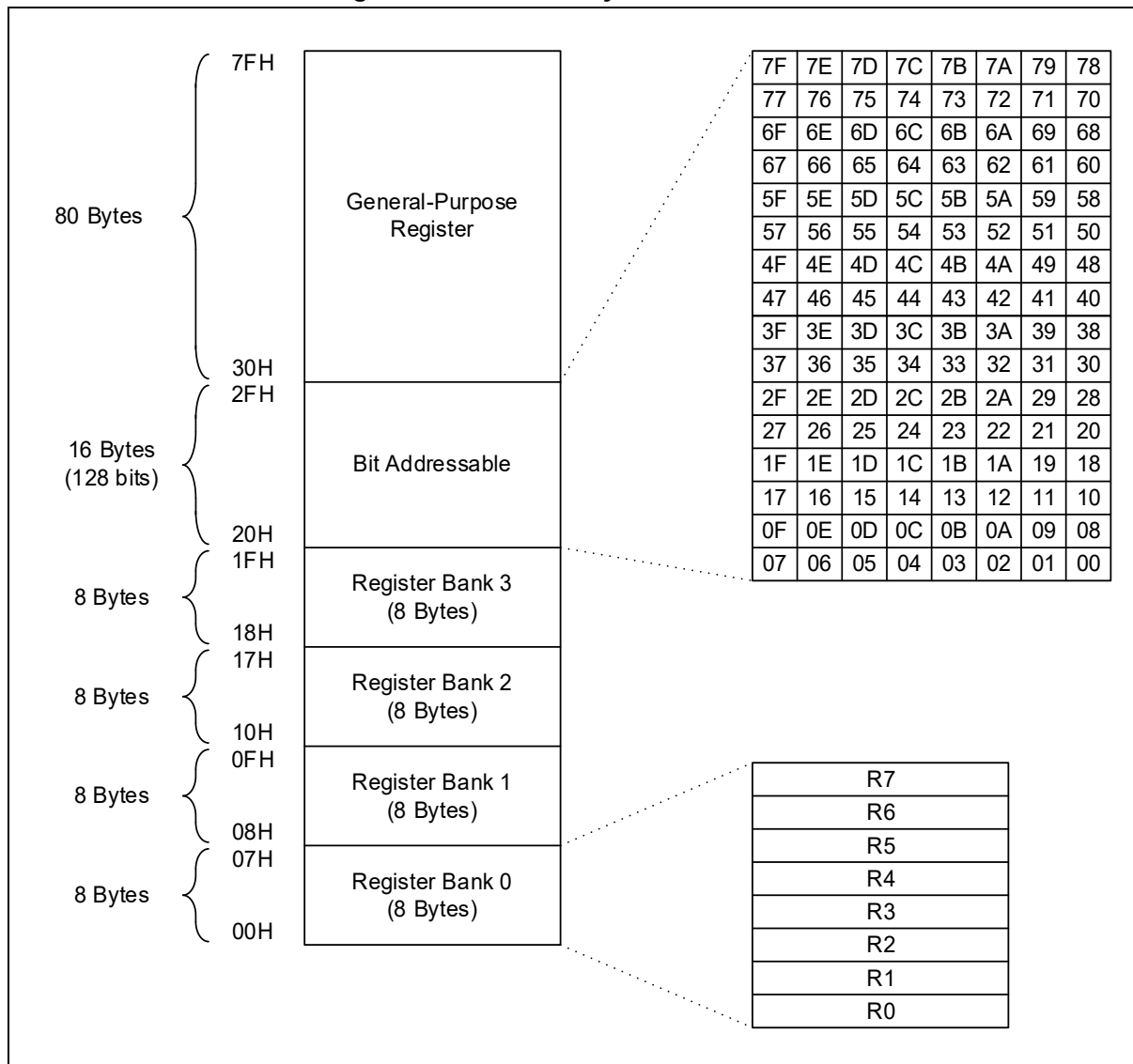


The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 12. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instructions set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Entire bytes in the lower 128 bytes can be accessed by either direct or indirect addressing, while the upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

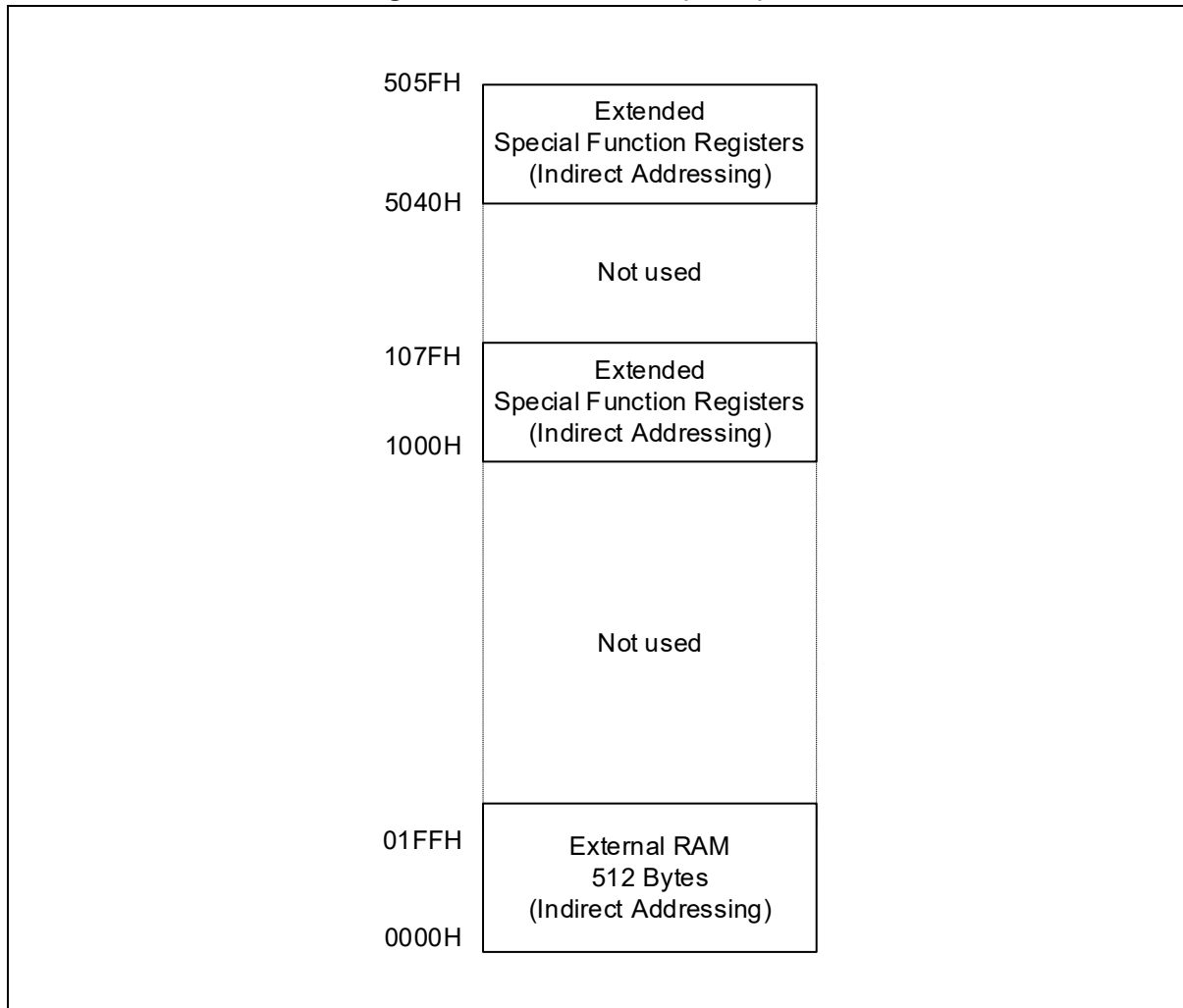
Figure 12. Lower 128 Bytes Internal RAM



4.4 Extended SFR and Data Memory Area

MC96F8316P has 512 bytes XRAM and XSFR registers. Extended SFR area has no relation with RAM nor Flash. This area can be read or written to by using SFR in 8-bit unit.

Figure 13. Extended SFR (XSFR) Area



4.5 SFR Map

In this section, information of SFR map and map summaries are described through Table 5, Table 6, Table 7, and Table 8.

4.5.1 SFR Map Summary

Table 5. SFR Map Summary

– Reserved M8051 compatible

	00H/08H ⁽¹⁾	01H/09H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
0F8H	IP1	–	FSADRH	FSADRM	FSADRL	FIDR	FMCR	–
0F0H	B	I2CSAR1	ADWRCR0	ADWRCR1	ADWRCR2	ADWRCR3	ADWCRL	ADWCRH
0E8H	RSTFR	I2CCR	I2CSR	I2CSAR0	I2CDR	I2CSDHR	I2CSCLR	I2CSCHR
0E0H	ACC	FCDIN	UART0CR1	UART0CR2	UART0CR3	UART0ST	UART0BD	UART0DR
0D8H	LVRCR	–	–	–	ADWIFRL	ADWIFRH	P03DB	P12DB
0D0H	PSW	–	P2FSR	P0FSR	P1FSRL	P1FSRH	P3FSRL	P3FSRH
0C8H	OSCCR	–	UART1CR1	UART1CR2	UART1CR3	UART1ST	UART1BD	UART1DR
0C0H	EIFLAG0	P3IO	T2CRL	T2CRH	T2ADRL	T2ADRH	T2BDRL	T2BDRH
0B8H	IP	P2IO	T1CRL	T1CRH	T1ADRL	T1ADRH	T1BDRL	T1BDRH
0B0H	EIFLAG1	P1IO	T0CR	T0CNT	TODR/ TOCDR	SPICR	SPIDR	SPISR
0A8H	IE	IE1	IE2	IE3	P0PU	P1PU	P2PU	P3PU
0A0H	IIFLAG	P0IO	EO	–	EIPOL0L	EIPOL0H	EIPOL1	EIPOL2
98H	P3	–	–	–	ADCCRL	ADCCRH	ADCDRL	ADCDRH
90H	P2	P0OD	P1OD	P2OD	P3OD	–	WTCR	BUZDR
88H	P1	WTDR/ WTCNT	SCCR	BITCR	BITCNT	WDTCR	WDTR/ WDCNT	BUZDR
80H	P0	SP	DPL	DPH	DPL1	DPH1	LVICR	PCON

NOTE:

1. Registers 00H/08H are bit-addressable except OSCCR.

4.5.2 Extended SFR Map Summary

Table 6. XSFR Map Summary

-	Reserved
---	----------

	00H/8H	01H/9H	02H/0AH	03H/0BH	04H/0CH	05H/0DH	06H/0EH	07H/0FH
5058H	FCDRL	-	-	-	-	-	-	-
5050H	FCSARH	FCEARH	FCSARM	FCEARM	FCSARL	FCEARL	FCCR	FCDRH
.....	-	-	-	-	-	-	-	-
5040H	USERMCR	USERMSSR	USERMIDR	-	-	-	-	-
.....	-	-	-	-	-	-	-	-
1068H	UNIQUEID8	UNIQUEID9	UNIQUEID10	UNIQUEID11	UNIQUEID12	UNIQUEID13	UNIQUEID14	UNIQUEID15
1060H	UNIQUEID0	UNIQUEID1	UNIQUEID2	UNIQUEID3	UNIQUEID4	UNIQUEID5	UNIQUEID6	UNIQUEID7
.....	-	-	-	-	-	-	-	-
1038H	XTFLSR	-	-	-	-	-	-	-
.....	-	-	-	-	-	-	-	-
1010H	-	-	-	-	-	-	T2CAPL	T2CAPH
1008H	-	-	-	-	-	-	T1CAPL	T1CAPH
1000H	-	-	-	-	-	-	-	-

4.5.3 SFR Map

Table 7. SFR Map

Address	Function	Symbol	R/W	@ Reset								
				7	6	5	4	3	2	1	0	
80H	P0 Data Register	P0	R/W	–	0	0	0	0	0	0	0	0
81H	Stack Pointer	SP	R/W	0	0	0	0	0	1	1	1	1
82H	Data Pointer Register Low	DPL	R/W	0	0	0	0	0	0	0	0	0
83H	Data Pointer Register High	DPH	R/W	0	0	0	0	0	0	0	0	0
84H	Data Pointer Register Low 1	DPL1	R/W	0	0	0	0	0	0	0	0	0
85H	Data Pointer Register High 1	DPH1	R/W	0	0	0	0	0	0	0	0	0
86H	Low Voltage Indicator Control Register	LVICR	R/W	–	–	0	0	0	0	0	0	0
87H	Power Control Register	PCON	R/W	–	–	–	–	–	–	0	0	0
88H	P1 Data Register	P1	R/W	0	0	0	0	0	0	0	0	0
89H	Watch Timer Data Register	WTDR	W	0	1	1	1	1	1	1	1	1
89H	Watch Timer Counter Register	WTCNT	R	–	0	0	0	0	0	0	0	0
8AH	System and Clock Control Register	SCCR	R/W	–	–	–	–	–	–	0	0	0
8BH	BIT Control Register	BITCR	R/W	0	0	0	–	0	0	0	1	1
8CH	Basic Interval Timer Counter Register	BITCNT	R	0	0	0	0	0	0	0	0	0
8DH	Watchdog Timer Control Register	WDTCR	R/W	0	0	0	–	–	–	0	0	0
8EH	Watchdog Timer Data Register	WDTDR	W	1	1	1	1	1	1	1	1	1
8EH	Watchdog Timer Counter Register	WDCNT	R	0	0	0	0	0	0	0	0	0
8FH	Buzzer Data Register	BUZDR	R/W	1	1	1	1	1	1	1	1	1
90H	P2 Data Register	P2	R/W	–	0	0	0	0	0	0	0	0
91H	P0 Open-drain Selection Register	P0OD	R/W	–	0	0	0	0	0	0	0	0
92H	P1 Open-drain Selection Register	P1OD	R/W	0	0	0	0	0	0	0	0	0
93H	P2 Open-drain Selection Register	P2OD	R/W	–	0	0	0	0	0	0	0	0
94H	P3 Open-drain Selection Register	P3OD	R/W	0	0	0	0	0	0	0	0	0
95H	Reserved	–	–	–								
96H	Watch Timer Control Register	WTCR	R/W	0	–	–	0	0	0	0	0	0
97H	BUZZER Control Register	BUZCR	R/W	–	–	–	–	0	0	0	0	0

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset								
				7	6	5	4	3	2	1	0	
98H	P3 Data Register	P3	R/W	0	0	0	0	0	0	0	0	0
99H	Reserved	–	–	–								
9AH	Reserved	–	–	–								
9BH	Reserved	–	–	–								
9CH	A/D Converter Control Low Register	ADCCRL	R/W	0	0	0	0	0	0	0	0	0
9DH	A/D Converter Control High Register	ADCCRH	R/W	0	–	–	0	0	0	0	0	0
9EH	A/D Converter Data Low Register	ADCDRL	R	x	x	x	x	x	x	x	x	x
9FH	A/D Converter Data High Register	ADCDRH	R	x	x	x	x	x	x	x	x	x
A0H	Internal Interrupt Flag Register	IIFLAG	R/W	–	–	–	–	–	0	0	0	0
A1H	P0 Direction Register	P0IO	R/W	–	0	0	0	0	0	0	0	0
A2H	Extended Operation Register	EO	R/W	–	–	–	0	–	0	0	0	0
A3H	Reserved	–	–	–								
A4H	External Interrupt Polarity 0 Low Register	EIPOL0L	R/W	0	0	0	0	0	0	0	0	0
A5H	External Interrupt Polarity 0 High Register	EIPOL0H	R/W	–	–	0	0	0	0	0	0	0
A6H	External Interrupt Polarity 1 Register	EIPOL1	R/W	–	–	0	0	0	0	0	0	0
A7H	External Interrupt Polarity 2 Register	EIPOL2	R/W	0	0	0	0	0	0	0	0	0
A8H	Interrupt Enable Register	IE	R/W	0	–	0	0	0	0	0	0	0
A9H	Interrupt Enable Register 1	IE1	R/W	–	–	0	0	0	0	0	0	0
AAH	Interrupt Enable Register 2	IE2	R/W	–	–	0	–	0	0	0	0	0
ABH	Interrupt Enable Register 3	IE3	R/W	–	–	–	0	0	0	0	0	0
ACH	P0 Pull-up Resistor Selection Register	P0PU	R/W	–	0	0	0	0	0	0	0	0
ADH	P1 Pull-up Resistor Selection Register	P1PU	R/W	0	0	0	0	0	0	0	0	0
AEH	P2 Pull-up Resistor Selection Register	P2PU	R/W	–	0	0	0	0	0	0	0	0
AFH	P3 Pull-up Resistor Selection Register	P3PU	R/W	0	0	0	0	0	0	0	0	0

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset								
				7	6	5	4	3	2	1	0	
B0H	External Interrupt Flag 1 Register	EIFLAG1	R/W	–	0	0	0	0	0	0	0	0
B1H	P1 Direction Register	P1IO	R/W	0	0	0	0	0	0	0	0	0
B2H	Timer 0 Control Register	T0CR	R/W	0	–	0	0	0	0	0	0	0
B3H	Timer 0 Counter Register	T0CNT	R	0	0	0	0	0	0	0	0	0
B4H	Timer 0 Data Register	T0DR	R/W	1	1	1	1	1	1	1	1	1
B4H	Timer 0 Capture Data Register	T0CDR	R	0	0	0	0	0	0	0	0	0
B5H	SPI Control Register	SPICR	R/W	0	0	0	0	0	0	0	0	0
B6H	SPI Data Register	SPIDR	R/W	0	0	0	0	0	0	0	0	0
B7H	SPI Status Register	SPISR	R/W	0	0	0	–	0	0	–	–	–
B8H	Interrupt Priority Register	IP	R/W	–	–	0	0	0	0	0	0	0
B9H	P2 Direction Register	P2IO	R/W	–	0	0	0	0	0	0	0	0
BAH	Timer 1 Control Low Register	T1CRL	R/W	0	0	0	0	–	0	0	0	0
BBH	Timer 1 Control High Register	T1CRH	R/W	0	–	0	0	–	–	–	–	0
BCH	Timer 1 A Data Low Register	T1ADRL	R/W	1	1	1	1	1	1	1	1	1
BDH	Timer 1 A Data High Register	T1ADRH	R/W	1	1	1	1	1	1	1	1	1
BEH	Timer 1 B Data Low Register	T1BDRL	R/W	1	1	1	1	1	1	1	1	1
BFH	Timer 1 B Data High Register	T1BDRH	R/W	1	1	1	1	1	1	1	1	1
C0H	External Interrupt Flag 0 Register	EIFLAG0	R/W	–	0	0	0	0	0	0	0	0
C1H	P3 Direction Register	P3IO	R/W	0	0	0	0	0	0	0	0	0
C2H	Timer 2 Control Low Register	T2CRL	R/W	0	0	0	0	0	0	0	0	0
C3H	Timer 2 Control High Register	T2CRH	R/W	0	–	0	0	–	–	–	–	0
C4H	Timer 2 A Data Low Register	T2ADRL	R/W	1	1	1	1	1	1	1	1	1
C5H	Timer 2 A Data High Register	T2ADRH	R/W	1	1	1	1	1	1	1	1	1
C6H	Timer 2 B Data Low Register	T2BDRL	R/W	1	1	1	1	1	1	1	1	1
C7H	Timer 2 B Data High Register	T2BDRH	R/W	1	1	1	1	1	1	1	1	1
C8H	Oscillator Control Register	OSCCR	R/W	–	–	0	0	1	0	0	0	0
C9H	Reserved	–	–	–								
CAH	UART1 Control Register 1	UART1CR1	R/W	–	–	0	0	0	0	0	0	–
CBH	UART1 Control Register 2	UART1CR2	R/W	0	0	0	0	0	0	0	0	0
CCH	UART1 Control Register 3	UART1CR3	R/W	–	0	–	–	–	0	0	0	0
CDH	UART1 Status Register	UART1ST	R/W	1	0	0	0	0	0	0	0	0
CEH	UART1 Baud Rate Generation Register	UART1BD	R/W	1	1	1	1	1	1	1	1	1
CFH	UART1 Data Register	UART1DR	R/W	0	0	0	0	0	0	0	0	0

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset								
				7	6	5	4	3	2	1	0	
D0H	Program Status Word Register	PSW	R/W	0	0	0	0	0	0	0	0	0
D1H	Reserved	–	–	–								
D2H	P2 Function Selection Register	P2FSR	R/W	–	–	–	–	–	–	0	0	
D3H	P0 Function Selection Register	P0FSR	R/W	0	0	0	0	0	0	0	0	
D4H	P1 Function Selection Low Register	P1FSRL	R/W	0	0	0	0	0	0	0	0	
D5H	P1 Function Selection High Register	P1FSRH	R/W	–	0	0	0	0	0	0	0	
D6H	P3 Function Selection Low Register	P3FSRL	R/W	–	–	0	0	0	0	0	0	
D7H	P3 Function Selection High Register	P3FSRH	R/W	–	–	–	–	0	0	0	0	
D8H	Low Voltage Reset Control Register	LVRCR	R/W	0	–	–	0	0	0	0	0	
D9H	Reserved	–	–	–								
DAH	Reserved	–	–	–								
DBH	Reserved	–	–	–								
DCH	ADC Wake-up Interrupt Flag Low Register	ADWIFRL	R/W	0	0	0	0	0	0	0	0	
DDH	ADC Wake-up Interrupt Flag High Register	ADWIFRH	R/W	–	0	0	0	0	0	0	0	
DEH	P0/P3 Debounce Enable Register	P03DB	R/W	0	0	0	0	0	0	0	0	
DFH	P1/P2 Debounce Enable Register	P12DB	R/W	0	0	0	0	0	0	0	0	
E0H	Accumulator A Register	ACC	R/W	0	0	0	0	0	0	0	0	
E1H	Flash CRC Data In Register	FCDIN	R/W	0	0	0	0	0	0	0	0	
E2H	UART0 Control Register 1	UART0CR1	R/W	–	–	0	0	0	0	0	–	
E3H	UART0 Control Register 2	UART0CR2	R/W	0	0	0	0	0	0	0	0	
E4H	UART0 Control Register 3	UART0CR3	R/W	–	0	–	–	–	0	0	0	
E5H	UART0 Status Register	UART0ST	R/W	1	0	0	0	0	0	0	0	
E6H	UART0 Baud Rate Generation Register	UART0BD	R/W	1	1	1	1	1	1	1	1	
E7H	UART0 Data Register	UART0DR	R/W	0	0	0	0	0	0	0	0	

Table 7. SFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0
E8H	Reset Flag Register	RSTFR	R/W	1	x	0	–	x	–	–	–
E9H	I2C Control Register	I2CCR	R/W	0	0	0	0	0	0	0	0
EAH	I2C Status Register	I2CSR	R/W	0	0	0	0	0	0	0	0
EBH	I2C Slave Address 0 Register	I2CSAR0	R/W	0	0	0	0	0	0	0	0
ECH	I2C Data Register	I2CDR	R/W	0	0	0	0	0	0	0	0
EDH	I2C SDA Hold Time Register	I2CSDHR	R/W	0	0	0	0	0	0	0	1
EEH	I2C SCL Low Period Register	I2CSCLR	R/W	0	0	1	1	1	1	1	1
EFH	I2C SCL High Period Register	I2CSCHR	R/W	0	0	1	1	1	1	1	1
F0H	B Register	B	R/W	0	0	0	0	0	0	0	0
F1H	I2C Slave Address 1 Register	I2CSAR1	R/W	0	0	0	0	0	0	0	0
F2H	ADC Wake-up Resistor Control Register 0	ADWRCR0	R/W	0	0	0	0	0	0	0	0
F3H	ADC Wake-up Resistor Control Register 1	ADWRCR1	R/W	0	0	0	0	0	0	0	0
F4H	ADC Wake-up Resistor Control Register 2	ADWRCR2	R/W	0	0	0	0	0	0	0	0
F5H	ADC Wake-up Resistor Control Register 3	ADWRCR3	R/W	–	–	0	0	0	0	0	0
F6H	ADC Wake-up Control Low Register	ADWCRL	R/W	0	0	0	0	0	0	0	0
F7H	ADC Wake-up Control High Register	ADWCRH	R/W	–	0	0	0	0	0	0	0
F8H	Interrupt Priority Register 1	IP1	R/W	–	–	0	0	0	0	0	0
F9H	Reserved	–	–	–							
FAH	Flash Sector Address High Register	FSADRH	R/W	–	–	–	–	0	0	0	0
FBH	Flash Sector Address Middle Register	FSADRM	R/W	0	0	0	0	0	0	0	0
FCH	Flash Sector Address Low Register	FSADRL	R/W	0	0	0	0	0	0	0	0
FDH	Flash Identification Register	FIDR	R/W	0	0	0	0	0	0	0	0
FEH	Flash Mode Control Register	FMCR	R/W	0	–	–	–	–	0	0	0
FFH	Reserved	–	–	–							

4.5.4 Extended SFR Map

Table 8. XSFR Map

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0

100EH	Timer 1 Capture Data Low Register	T1CAPL	R	0	0	0	0	0	0	0	0
100FH	Timer 1 Capture Data High Register	T1CAPH	R	0	0	0	0	0	0	0	0

1016H	Timer 2 Capture Data Low Register	T2CAPL	R	0	0	0	0	0	0	0	0
1017H	Timer 2 Capture Data High Register	T2CAPH	R	0	0	0	0	0	0	0	0

1038H	X-tal Filter Selection Register	XTFLSR	R/W	0	0	0	0	0	0	0	0

1060H	Unique ID Register 0	UNIQUEID0	R	x	x	x	x	x	x	x	x
1061H	Unique ID Register 1	UNIQUEID1	R	x	x	x	x	x	x	x	x
1062H	Unique ID Register 2	UNIQUEID2	R	x	x	x	x	x	x	x	x
1063H	Unique ID Register 3	UNIQUEID3	R	x	x	x	x	x	x	x	x
1064H	Unique ID Register 4	UNIQUEID4	R	x	x	x	x	x	x	x	x
1065H	Unique ID Register 5	UNIQUEID5	R	x	x	x	x	x	x	x	x
1066H	Unique ID Register 6	UNIQUEID6	R	x	x	x	x	x	x	x	x
1067H	Unique ID Register 7	UNIQUEID7	R	x	x	x	x	x	x	x	x
1068H	Unique ID Register 8	UNIQUEID8	R	x	x	x	x	x	x	x	x
1069H	Unique ID Register 9	UNIQUEID9	R	x	x	x	x	x	x	x	x
106AH	Unique ID Register 10	UNIQUEID10	R	x	x	x	x	x	x	x	x
106BH	Unique ID Register 11	UNIQUEID11	R	x	x	x	x	x	x	x	x
106CH	Unique ID Register 12	UNIQUEID12	R	x	x	x	x	x	x	x	x
106DH	Unique ID Register 13	UNIQUEID13	R	x	x	x	x	x	x	x	x
106EH	Unique ID Register 14	UNIQUEID14	R	x	x	x	x	x	x	x	x
106FH	Unique ID Register 15	UNIQUEID15	R	x	x	x	x	x	x	x	x

Table 8. XSFR Map (continued)

Address	Function	Symbol	R/W	@ Reset							
				7	6	5	4	3	2	1	0

5040H	User Memory Control Register	USERMCR	R/W	0	0	0	0	0	0	0	0
5041H	User Memory Sector Selection Register	USERMSSR	R/W	0	0	0	0	0	0	0	0
5042H	User Memory Identification Register	USERMIDR	R/W	0	0	0	0	0	0	0	0

5050H	Flash CRC Start Address High Register	FCSARH	R/W	-	-	-	-	-	-	-	0
5051H	Flash CRC End Address High Register	FCEARH	R/W	-	-	-	-	-	-	-	0
5052H	Flash CRC Start Address Middle Register	FCSARM	R/W	0	0	0	0	0	0	0	0
5053H	Flash CRC End Address Middle Register	FCEARM	R/W	0	0	0	0	0	0	0	0
5054H	Flash CRC Start Address Low Register	FCSARL	R/W	0	0	0	0	0	0	0	0
5055H	Flash CRC End Address Low Register	FCEARL	R/W	0	0	0	0	1	1	1	1
5056H	Flash CRC Control Register	FCCR	R/W	0	0	0	-	0	0	0	0
5057H	Flash CRC Data High Register	FCDRH	R	1	1	1	1	1	1	1	1
5058H	Flash CRC Data Low Register	FCDRL	R	1	1	1	1	1	1	1	1

5. Ports

5.1 I/O Ports

MC96F8316P has four groups of I/O ports, P0, P1, P2 and P3. Each port can be easily configured as an input pin, an output, or an internal pull up and open-drain pin by software.

The port configuration pursues to meet various system configurations and design requirements.

5.2 Port Description of P0

As a 7-bit I/O port, P0 controls the following registers:

- P0 data register (P0)
- P0 direction register (P0IO)
- P0/P3 debounce enable register (P03DB)
- P0 pull-up resistor selection register (P0PU)
- P0 open-drain selection register (P0OD)
- P0 Function selection register (P0FSR)

5.3 Port Description of P1

As an 8-bit I/O port, P1 controls the following registers:

- P1 data register (P1)
- P1 direction register (P1IO)
- P1 pull-up resistor selection register (P1PU)
- P1/P2 debounce enable register (P12DB)
- P1 open-drain selection register (P1OD)
- P1 Function selection registers (P1FSRH/P1FSRL)

5.4 Port Description of P2

As a 7-bit I/O port, P2 controls the following registers:

- P2 data register (P2)
- P2 direction register (P2IO)
- P2 pull-up resistor selection register (P2PU)
- P2 open-drain selection register (P2OD)
- P2 Function selection register (P2FSR)

5.5 Port Description of P3

As an 8-bit I/O port, P3 controls the following registers:

- P3 data register (P3)
- P3 direction register (P3IO)
- P3 pull-up resistor selection register (P3PU)
- P3 open-drain selection register (P3OD)
- P3 Function selection registers (P3FSRL/P3FSRH)

6. Interrupt Controller

Up to 22 interrupt sources are available in the MC96F8316P. Allowing software control, each interrupt source can be enabled by defining separate enable register bit associated with it. It can also have four levels of priority assigned. The non-maskable interrupt source is always enabled with a higher priority than any other interrupt sources and is not controllable by software.

The interrupt controller features the followings:

- Receives requests from 22 interrupt sources
- 6 group priority
- 4 priority levels
- Multi interrupt possibility
- If requests of different priority levels are received simultaneously, a request with higher priority level is served first.
- Each interrupt source can be controlled by an EA bit and an IEx bit
- Interrupt latency varies ranging from 3 to 9 machine cycles in a single interrupt system.

Non-maskable interrupt is always enabled, while maskable interrupts can be enabled through four pairs of interrupts enable registers (IE, IE1, IE2, and IE3). Each bit of the four registers can individually enable or disable a particular interrupt source. Especially bit 7 (EA) in the register IE provides overall control. It must be set to '1' to enable interrupts as described in the followings:

- When EA is set to '0' → all interrupts are disabled.
- When EA is set to '1' → a particular interrupt can be individually enabled or disabled by the associate bit of the interrupt enable registers.

EA is always cleared to '0' jumping to an interrupt service vector and set to '1' executing the [RETI] instruction. MC96F8316P supports a four-level priority scheme. Each maskable interrupt is individually assigned to one of the four levels according to IP and IP1.

Figure 14. Interrupt Group Priority Level

Interrupt Group	Highest Lowest				
	→				
0 (Bit0)	Interrupt 0	Interrupt 6	Interrupt 12	Interrupt 18	Highest Lowest
1 (Bit1)	Interrupt 1	Interrupt 7	Interrupt 13	Interrupt 19	
2 (Bit2)	Interrupt 2	Interrupt 8	Interrupt 14	Interrupt 20	
3 (Bit3)	Interrupt 3	Interrupt 9	Interrupt 15	Interrupt 21	
4 (Bit4)	Interrupt 4	Interrupt 10	Interrupt 16	Interrupt 22	
5 (Bit5)	Interrupt 5	Interrupt 11	Interrupt 17	Interrupt 23	

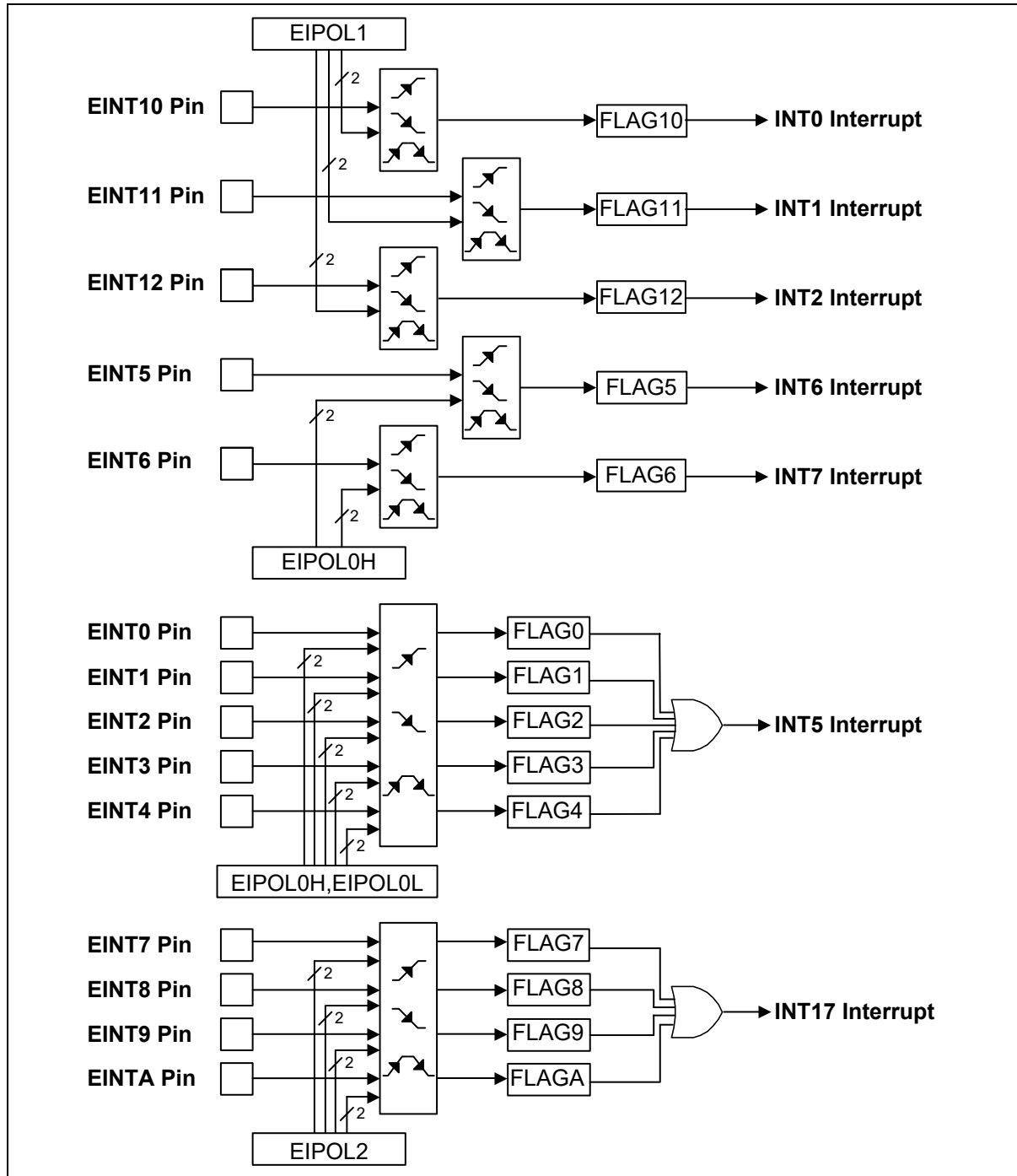
Figure 14 describes interrupt groups and their priority levels that is available for sharing interrupt priority. Priority of a group is set by 2 bits of Interrupt Priority (IP) registers: 1 bit from IP and another 1 bit from IP1.

Interrupt Service Routine serves an interrupt having higher priority first. If two requests of different priority levels are received simultaneously, the request with higher priority level is served prior to the lower one.

6.1 External Interrupt

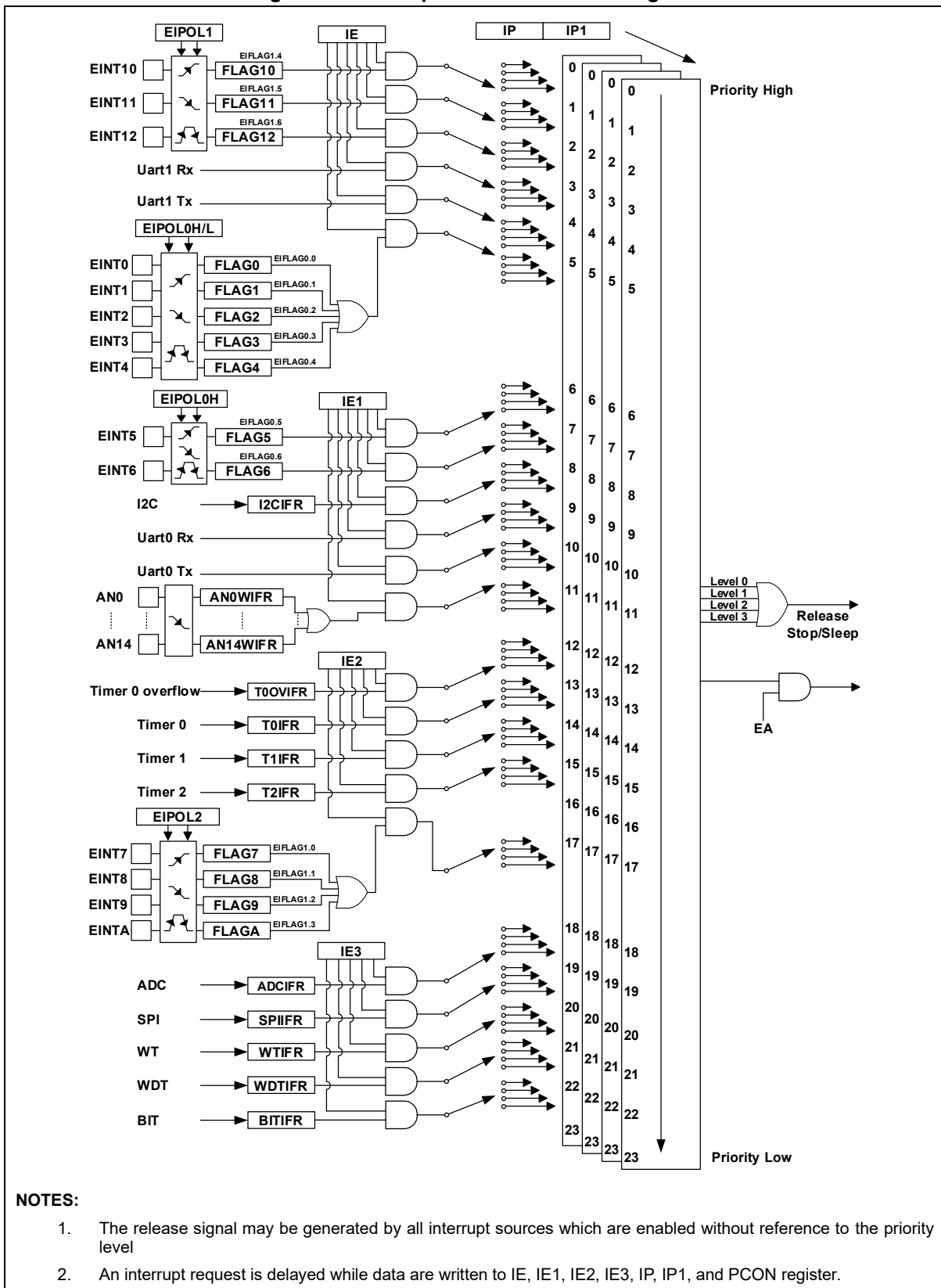
External interrupts on pins of INT0 to INT2, INT5 to INT7, INT17 receive various interrupt requests in accordance with the external interrupt polarity 0 registers (EIPOL0H/L), external interrupt polarity 1 register (EIPOL1) and external interrupt polarity 2 register (EIOPL2) as shown in Figure 15. Each external interrupt source has enable/disable bits. An external interrupt flag register (EIFLAG) provides the status of the external interrupts.

Figure 15. External Interrupt Description



6.2 Interrupt Controller Block Diagram

Figure 16. Interrupt Controller Block Diagram



In Figure 16, release signal for STOP and IDLE mode can be generated by all interrupt sources which are enabled without reference to priority level. An interrupt request will be delayed while data is written to one of the registers IE, IE1, IE2, IE3, IP, IP1, and PCON.

6.3 Interrupt Vector Table

When a certain interrupt occurs, a LCALL (Long Call) instruction pushes the contents of the PC (Program Counter) onto the stack and loads the appropriate vector address. CPU pauses from its current task for some time and processes the interrupt at the vector address.

The Interrupt controller supports 24 interrupt sources, and each interrupt source has a determined priority order as shown in Table 9.

Table 9. Interrupt Vector Address Table

Interrupt source	Symbol	Interrupt Enable Bit	Priority	Mask	Vector address
Hardware RESET	RESETB	–	0	Non-Maskable	0000H
External Interrupt 10	INT0	IE.0	1	Maskable	0003H
External Interrupt 11	INT1	IE.1	2	Maskable	000BH
External Interrupt 12	INT2	IE.2	3	Maskable	0013H
UART1 Rx Interrupt	INT3	IE.3	4	Maskable	001BH
UART1 Tx Interrupt	INT4	IE.4	5	Maskable	0023H
External Interrupt 0 – 4	INT5	IE.5	6	Maskable	002BH
External Interrupt 5	INT6	IE1.0	7	Maskable	0033H
External Interrupt 6	INT7	IE1.1	8	Maskable	003BH
I2C Interrupt	INT8	IE1.2	9	Maskable	0043H
UART0 Rx Interrupt	INT9	IE1.3	10	Maskable	004BH
UART0 Tx Interrupt	INT10	IE1.4	11	Maskable	0053H
ADC Wake-up Interrupt	INT11	IE1.5	12	Maskable	005BH
T0 Overflow Interrupt	INT12	IE2.0	13	Maskable	0063H
T0 Match Interrupt	INT13	IE2.1	14	Maskable	006BH
T1 Match Interrupt	INT14	IE2.2	15	Maskable	0073H
T2 Match Interrupt	INT15	IE2.3	16	Maskable	007BH
–	INT16	IE2.4	17	Maskable	0083H
External Interrupt 7 – A	INT17	IE2.5	18	Maskable	008BH
ADC Interrupt	INT18	IE3.0	19	Maskable	0093H
SPI Interrupt	INT19	IE3.1	20	Maskable	009BH
WT Interrupt	INT20	IE3.2	21	Maskable	00A3H
WDT Interrupt	INT21	IE3.3	22	Maskable	00ABH
BIT Interrupt	INT22	IE3.4	23	Maskable	00B3H
–	INT23	IE3.5	24	Maskable	00BBH

To execute the maskable interrupts, both EA bit and a corresponding bit of IEx associated with a specific interrupt source must be set to '1'.

When an interrupt request is received, a particular interrupt request flag is set to '1' and maintains its status until CPU accepts the interrupt.

After the interrupt acceptance, the interrupt request flag will be cleared automatically.

7. Clock Generator

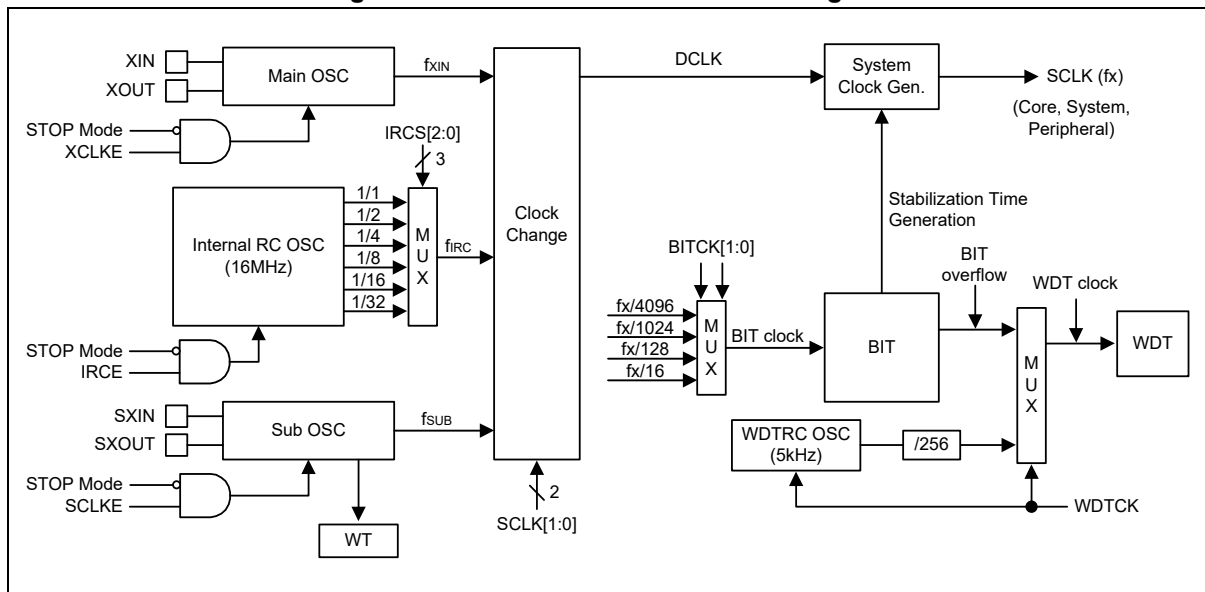
As shown in Figure 17, a clock generator produces basic clock pulses which provide a CPU and peripherals with a system clock. It contains a main/sub frequency clock oscillator. The main/sub clock operation can be easily obtained by attaching a crystal between the XIN/SXIN and XOUT/SXOUT pin, respectively. The main/sub clock can be also obtained from the external oscillator. In this case, it is necessary to put the external clock signal into the XIN/SXIN pin and open the XOUT/SXOUT pin. The default system clock is a 1MHz INT-RC oscillator and default division rate is sixteen. To stabilize the system internally, it is used 1MHz INT-RC oscillator on POR.

MC96F8316P incorporates four types of oscillators:

- Calibrated Internal RC Oscillator (16 MHz)
 - INT-RC OSC/32 (0.5 MHz)
 - INT-RC OSC/16 (1 MHz, default system clock)
 - INT-RC OSC/8 (2 MHz)
 - INT-RC OSC/4 (4 MHz)
 - INT-RC OSC/2 (8 MHz)
 - INT-RC OSC/1 (16 MHz)
- Main Crystal Oscillator (0.4~12 MHz)
- Sub Crystal Oscillator (32.768 kHz)
- Internal WDTRC Oscillator (5 kHz)

7.1 Clock Generator Block Diagram

Figure 17. Clock Generator in Block Diagram



8. Basic Interval Timer (BIT)

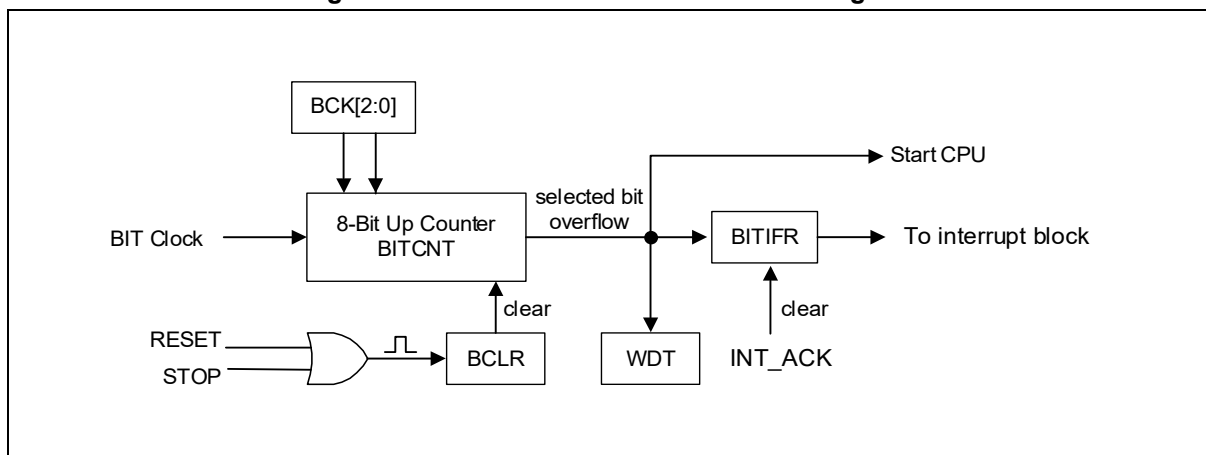
MC96F8316P has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting and provides a basic interval timer interrupt (BITIFR).

BIT of MC96F8316P features the followings:

- During Power On, BIT gives a stable clock generation time
- On exiting Stop mode, BIT gives a stable clock generation time
- As a timer, BIT generates a timer interrupt.

8.1 Basic Interval Timer Block Diagram

Figure 18. Basic Interval Timer in Block Diagram



9. Watchdog Timer (WDT)

Watchdog Timer (WDT) is used to rapidly detect CPU malfunctions such as endless looping caused by noise. In addition, it is used to resume the CPU in a normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the WDT is not being used for the detection of the CPU malfunctions, it can be used as a timer generating an interrupt at fixed intervals.

The WDT can be used in a free running 8-bit timer mode or in a Watchdog Timer mode by setting WDTRSON bit, which is WDTCR[6]. If '1' is written to WDTCR[5], WDT counter value is cleared and counts. After 1 machine cycle, this bit is cleared to '0' automatically.

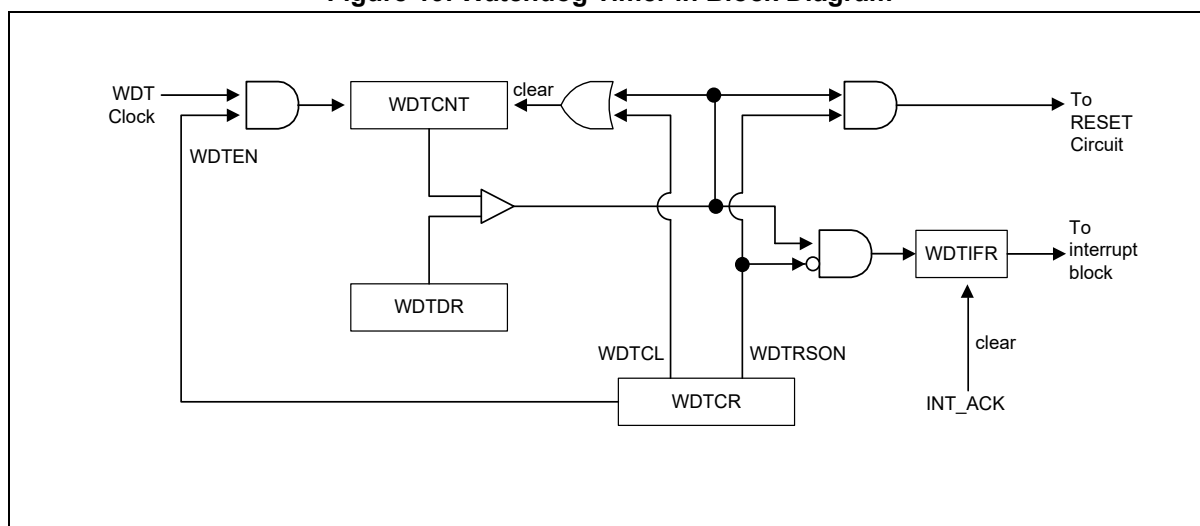
The WDT consists of an 8-bit binary counter and a watchdog timer data register. When the value of an 8-bit binary counter is equal to the 8 bits of WDCNT, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset of CPU in accordance with a bit WDTRSON.

The input clock source of Watchdog Timer is BIT overflow and WDTRC. The interval of watchdog timer interrupt is decided by the BIT overflow period and WDTDR set value. Equation of the WDT interrupt interval is described in the followings:

- WDT Interrupt Interval = (BIT Interrupt Interval) X (WDTDR Value+1)
- WDT Interrupt Interval = $256/f_{WDTRC} \times (WDTDR \text{ Value}+1)$ when WDTRC

9.1 Watchdog Timer Block Diagram

Figure 19. Watchdog Timer in Block Diagram



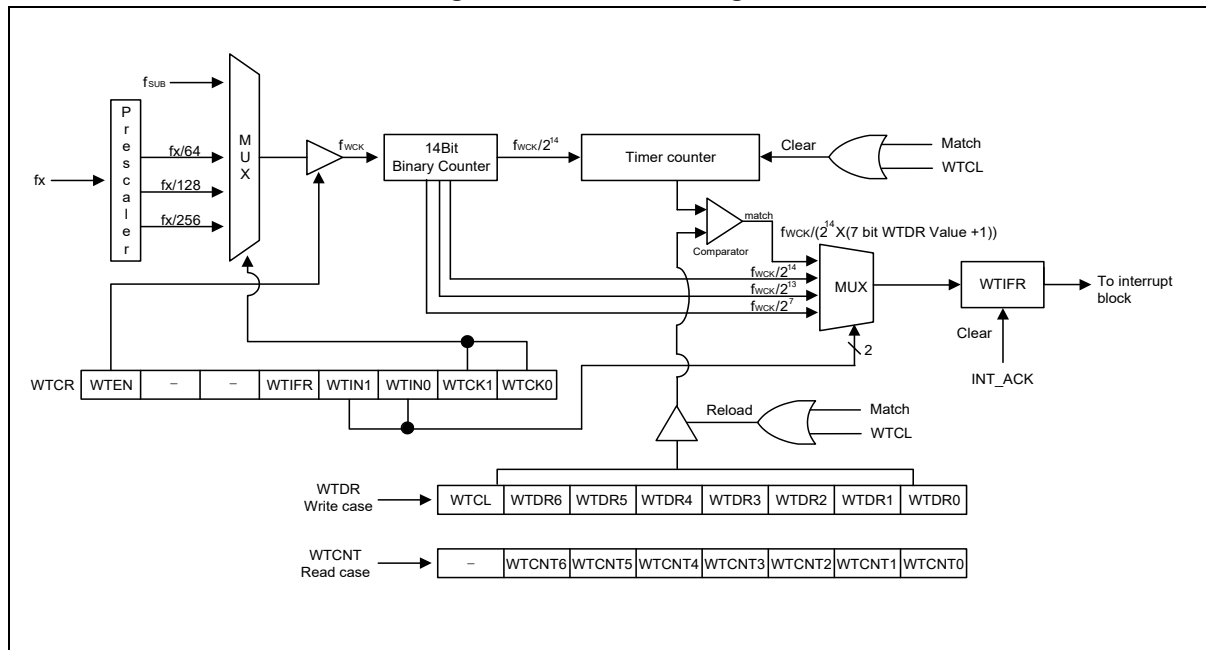
10. Watch Timer

The watch timer has the function for RTC (Real Time Clock) operation. It is generally used for RTC design. The internal structure of the watch timer consists of the clock source select circuit, timer counter circuit, output select circuit and watch timer control register.

To operate the watch timer, determine the input clock source, output interval and set WTEN to '1' in watch timer control register (WTCR). It can execute simultaneously or individually. To stop or reset WT, clear the WTEN bit in WTCR register.

Even if CPU is STOP mode, sub clock can be so alive that WT can continue the operation. The watch timer counter circuits may be composed of 21-bit counters which contain low 14-bit with binary counter and high 7-bit counter to raise resolution. In WTDR, it can control the WT clear and set interval value at write time and it can read 7-bit WT counter value at read time.

Figure 20. WT Block Diagram



11. TIMER 0

The 8-bit timer 0 consists of multiplexer, timer 0 counter register, timer 0 data register, timer 0 capture data register and timer 0 control register (T0CNT, T0DR, T0CDR, T0CR).

TIMER 0 operates in one of three operating modes:

- 8-bit capture mode
- 8-bit timer/counter mode
- 8-bit PWM output mode

Specifically in capture mode, data is captured into input capture data register (T0CDR) by EINT10. Timer 0 outputs the comparison result between counter and data register through T0O port in timer/counter mode. Timer 0 outputs PWM wave form through PWM0O port in the PPG mode).

A timer/counter 0 uses an internal clock or an external clock (EC0) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (T0CK[2:0]).

- Timer 0 clock sources: $fX/2$, 4, 8, 32, 128, 512, 2048 and EC0

Table 10. TIMER 0 Operating Modes

T0EN	P3FSRL[5]	T0MS[1:0]	T0CK[2:0]	Timer 0
1	1	00	XXX	8 Bit Timer/Counter Mode
1	0	1X	XXX	8 Bit Capture Mode
1	1	01	XXX	8 Bit PWM Mode

12. TIMER 1

A 16-bit timer 1 incorporates a multiplexer and eight registers such as timer 1 A data register high/low, timer 1 B data register high/low, timer 1 capture data register high/low, and timer 1 control register high/low (T1ADRH, T1ADRL, T1BDRH, T1BDRL, T1CAPH, T1CAPL, T1CRH, T1CRL).

TIMER 1 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into capture data register (T1CAPH/T1CAPL) by EINT11. Timer 1 outputs the comparison result between counter and data register through T1O port in timer/counter mode. Timer 1 outputs PWM wave form through PWM1O port in the PPG mode).

A timer/counter 1 uses an internal clock or an external clock (EC1) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (T1CK[2:0]).

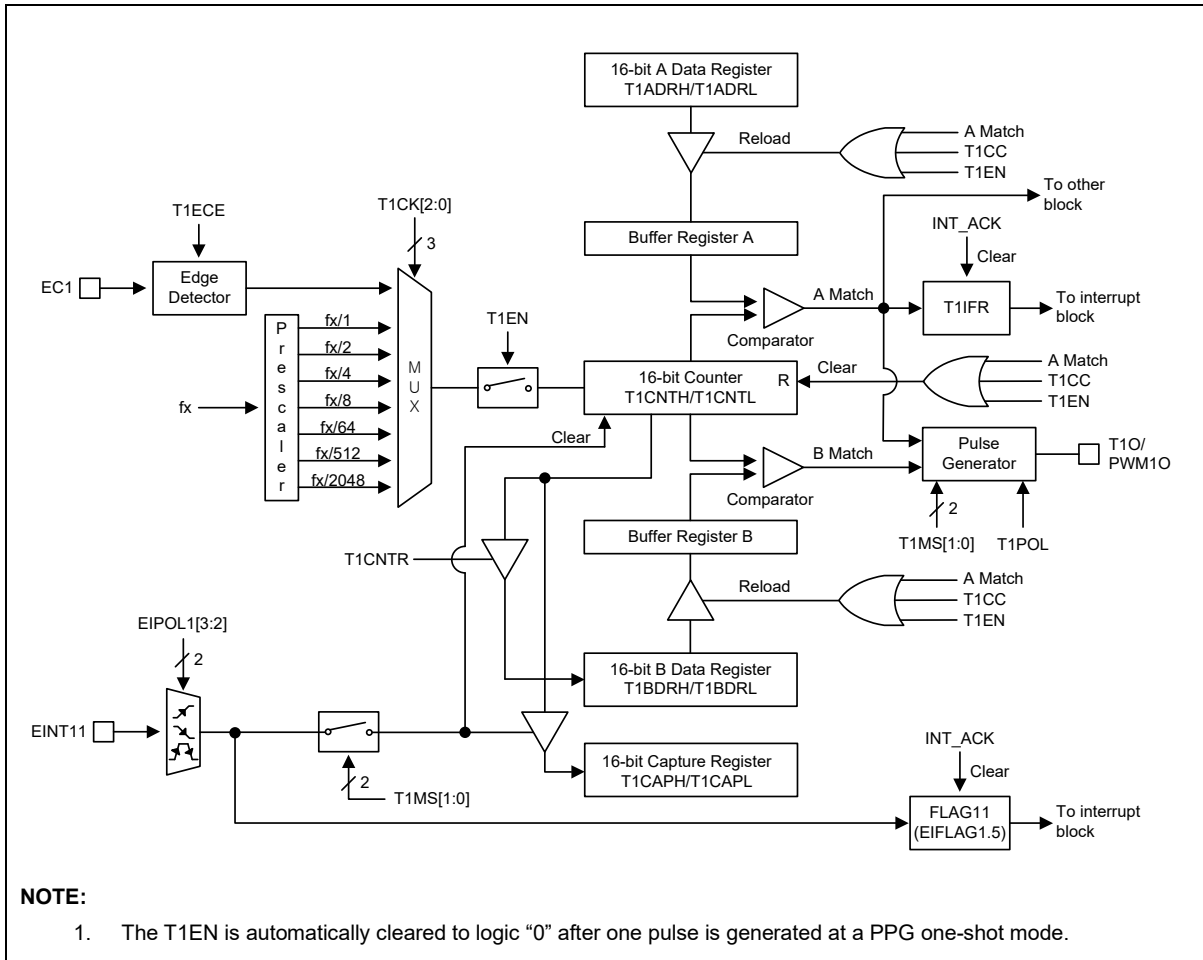
- Timer 1 clock sources: fX/1, 2, 4, 8, 64, 512, 2048 and ECn

Table 11. TIMER 1 Operating Modes

T1EN	P1FSRL[5:4]	T1MS[1:0]	T1CK[2:0]	Timer 1
1	01	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	01	10	XXX	16 Bit PPG Mode (One-shot Mode)
1	01	11	XXX	16 Bit PPG Mode (Repeat Mode)

12.1 Timer 1 Block Diagram

Figure 22. 16-bit Timer 1 in Block Diagram



13. TIMER 2

A 16-bit timer 2 incorporates a multiplexer and eight registers such as timer 2 A data register high/low, timer 2 B data register high/low, timer 2 capture data register high/low, and timer 2 control register high/low (T2ADRH, T2ADRL, T2BDRH, T2BDRL, T2CAPH, T2CAPL, T2CRH, T2CRL).

TIMER 2 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into capture data register (T2CAPH/T2CAPL) by EINT12. Timer 2 outputs the comparison result between counter and data register through T2O port in timer/counter mode. Timer 2 outputs PWM wave form through PWM2O port in the PPG mode).

A timer/counter 2 uses an internal clock or an external clock (EC2, T1 A Match) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (T2CK[2:0]).

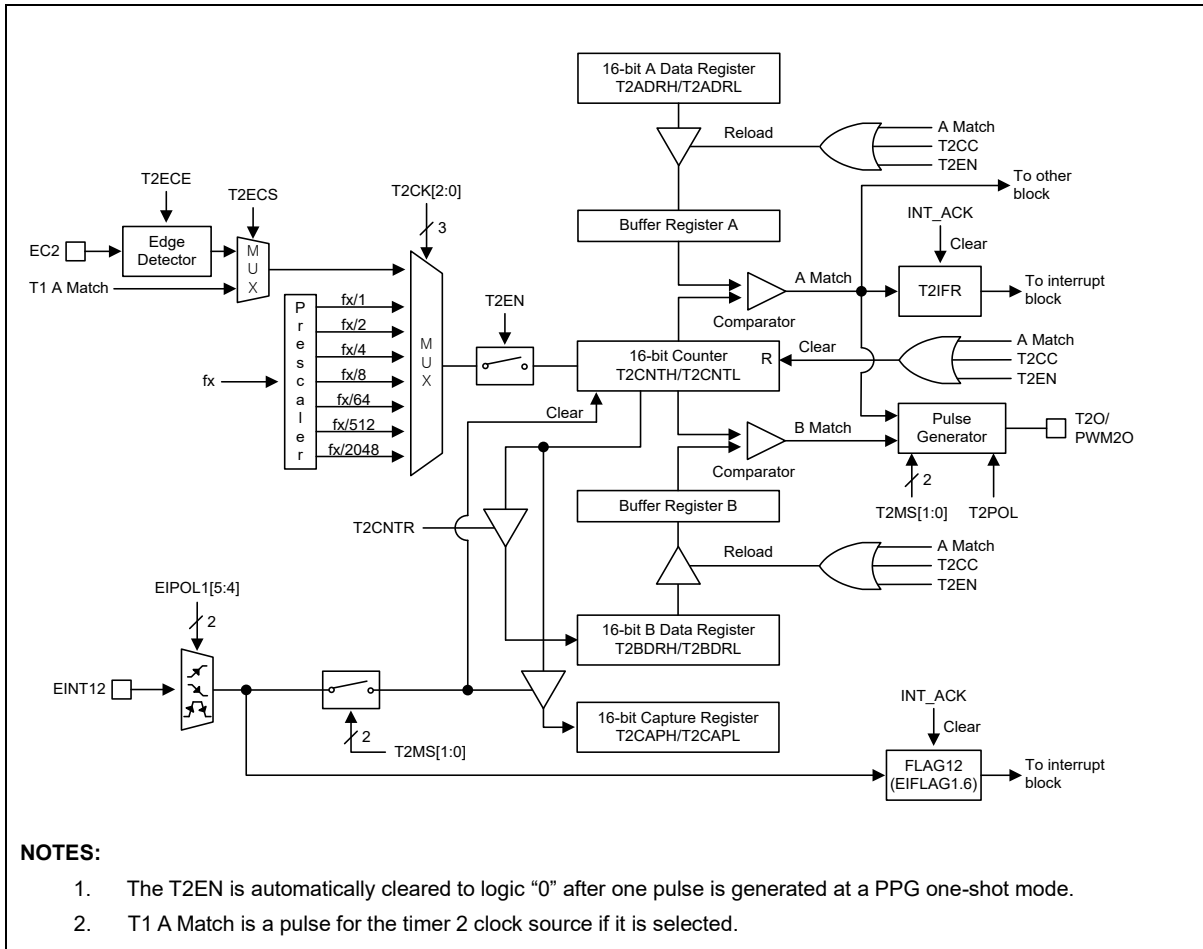
- Timer 2 clock sources: fX/1, 2, 4, 8, 64, 512, 2048 and ECn

Table 12. TIMER 2 Operating Modes

T2EN	P1FSRL[7:6]	T2MS[1:0]	T2CK[2:0]	Timer 2
1	01	00	XXX	16 Bit Timer/Counter Mode
1	00	01	XXX	16 Bit Capture Mode
1	01	10	XXX	16 Bit PPG Mode (One-shot Mode)
1	01	11	XXX	16 Bit PPG Mode (Repeat Mode)

13.1 Timer 2 Block Diagram

Figure 23. 16-bit Timer 2 in Block Diagram



14. Buzzer

The Buzzer consists of an 8-bit counter, buzzer data register (BUZDR) and buzzer control register (BUZCR). The Square Wave (61.035 Hz~125.0 kHz @8 MHz) is output through P11/BUZO pin. The buzzer data register (BUZDR) controls the buzzer frequency (look at the following expression). In buzzer control register (BUZCR), BUCK[2:0] selects source clock divided by prescaler.

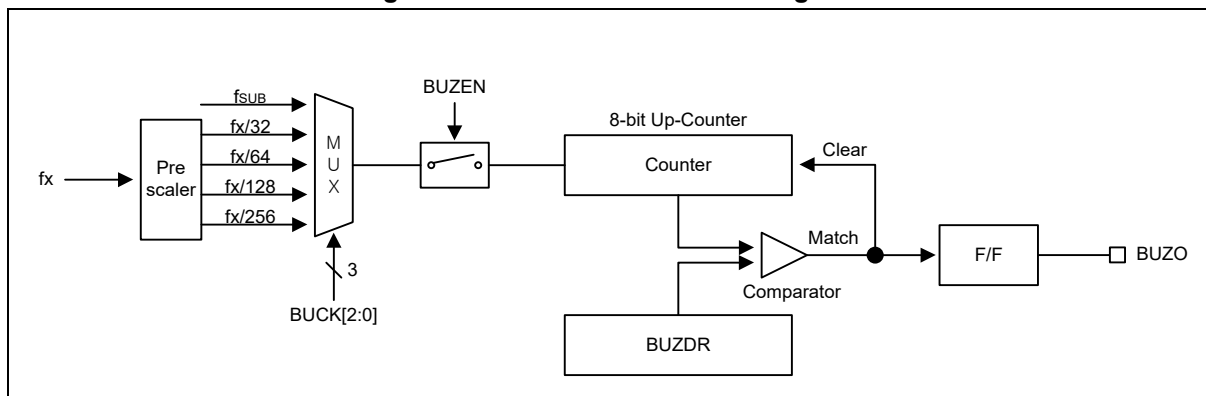
$$f_{\text{BUZ}}(\text{Hz}) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

Table 13. Buzzer Frequency at 8 MHz

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[3:1]=000	BUZCR[3:1]=001	BUZCR[3:1]=010	BUZCR[3:1]=011
0000_0000	125 kHz	62.5 kHz	31.25 kHz	15.625 kHz
0000_0001	62.5 kHz	31.25 kHz	15.625 kHz	7.812 kHz
...
1111_1101	492.126 Hz	246.063 Hz	123.031 Hz	61.515 Hz
1111_1110	490.196 Hz	245.098 Hz	122.549 Hz	61.274 Hz
1111_1111	488.281 Hz	244.141 Hz	122.07 Hz	61.035 Hz

14.1 Timer 3 Block Diagram

Figure 24. Buzzer Driver Block Diagram



15. 12-bit A/D Converter

Analog-to-Digital (A/D) converter allows conversion of an analog input signal to a corresponding 12-bit digital output. The A/D module has 15 analog inputs, and the output of the multiplexer becomes the input into the converter, which generates a result via successive approximation.

The A/D module incorporates twelve registers as listed in the following.

Each register can be selected for the corresponding channel by setting ADSEL[3:0]. When conversion is completed, two registers ADCDRH and ADCDRL contain the results of the conversion, the conversion status bit AFLAG is set to '1', and A/D interrupt is set. During the A/D conversion, AFLAG bit is read as '0'. Other registers are used to wake-up from Stop mode by falling edge of ANx input. ADWRCRx is Wake-up Resistor selection for ANx input, ADWCRH/L is Wake-up Enable bit for ANx.

- A/D converter control high register (ADCCRH)
- A/D converter control low register (ADCCRL)
- A/D converter data high register (ADCDRH)
- A/D converter data low register (ADCDRL)
- ADC wake-up resistor control register 0(ADWRCR0)
- ADC wake-up resistor control register 1(ADWRCR1)
- ADC wake-up resistor control register 2(ADWRCR2)
- ADC wake-up resistor control register 3(ADWRCR3)
- ADC wake-up resistor control high register(ADWCRH)
- ADC wake-up resistor control low register(ADWCRL)
- ADC wake-up interrupt flag high register(ADWIFRH)
- ADC wake-up interrupt flag low register(ADWIFRL)

15.1 ADC Block Diagram

Figure 25. 12-bit ADC Block Diagram

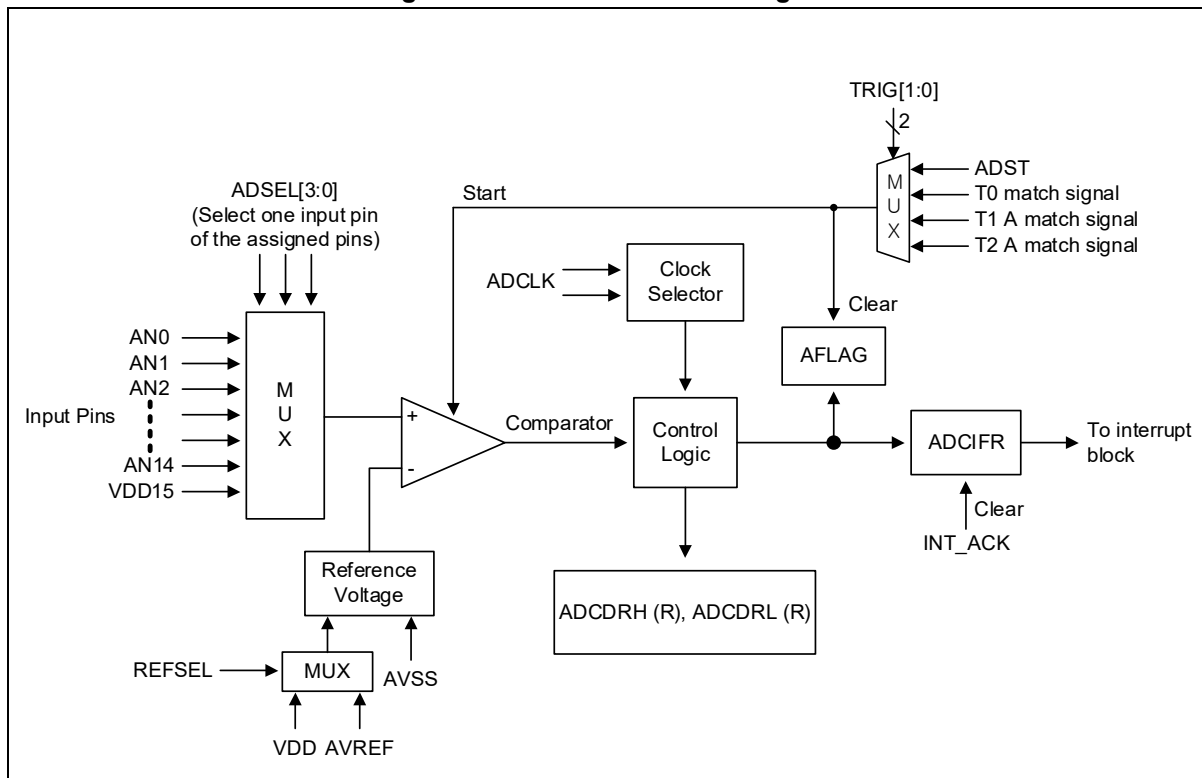


Figure 26. AD Analog Input Pin with Capacitor

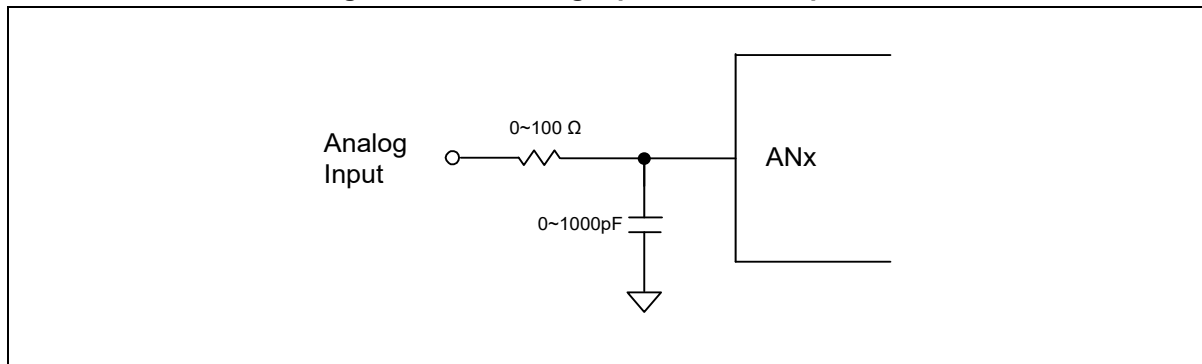


Figure 27. AD Power(AVREF) Pin with Capacitor

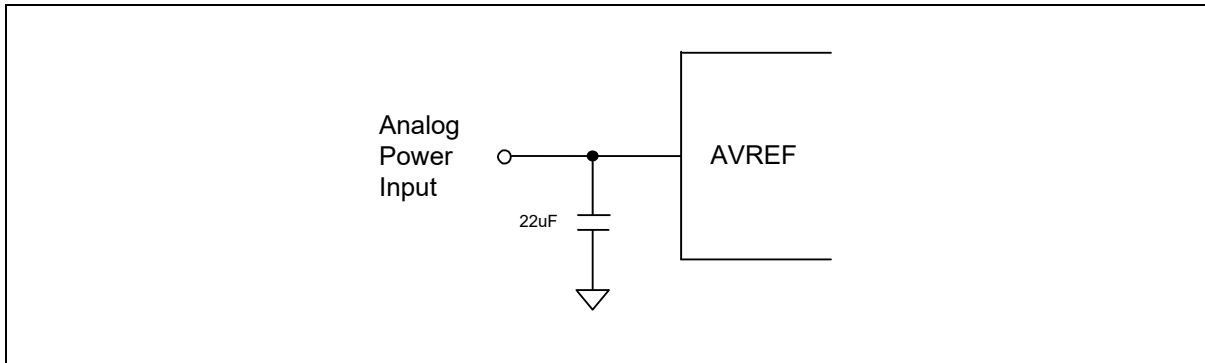
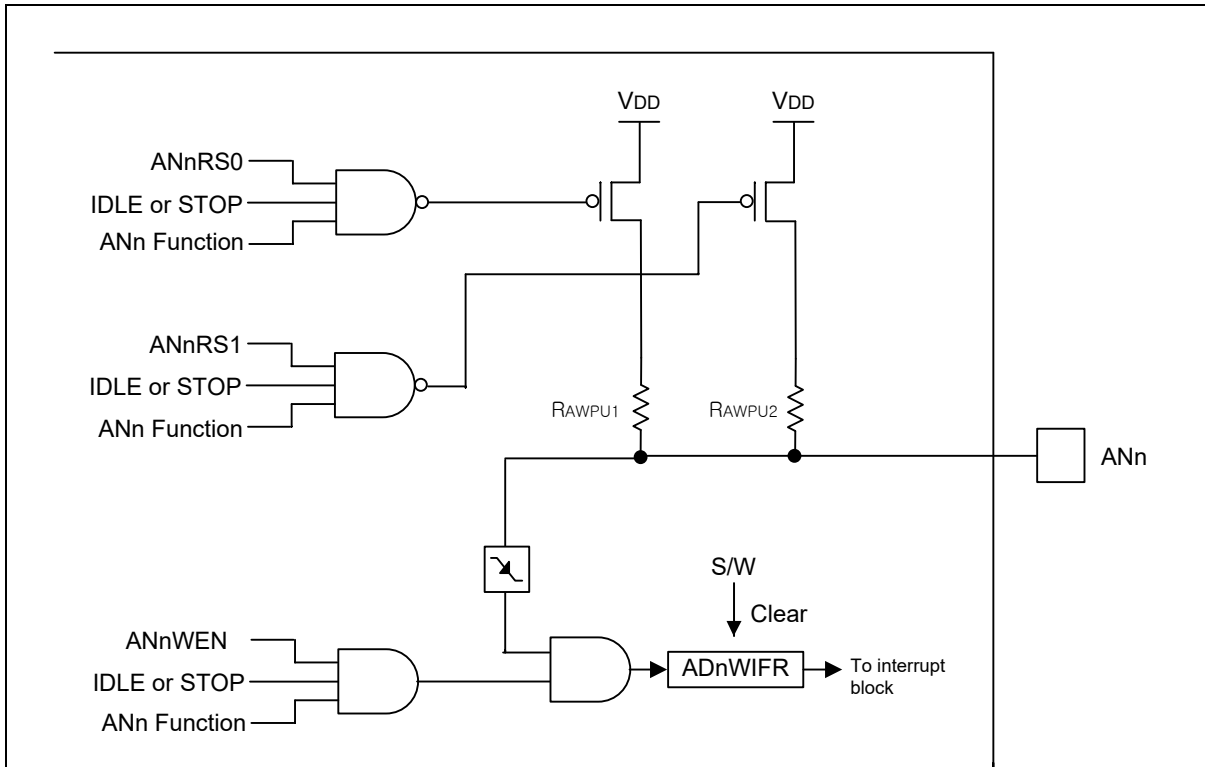


Figure 28. ADC Power-down Wake-up Function Block Diagram



NOTES:

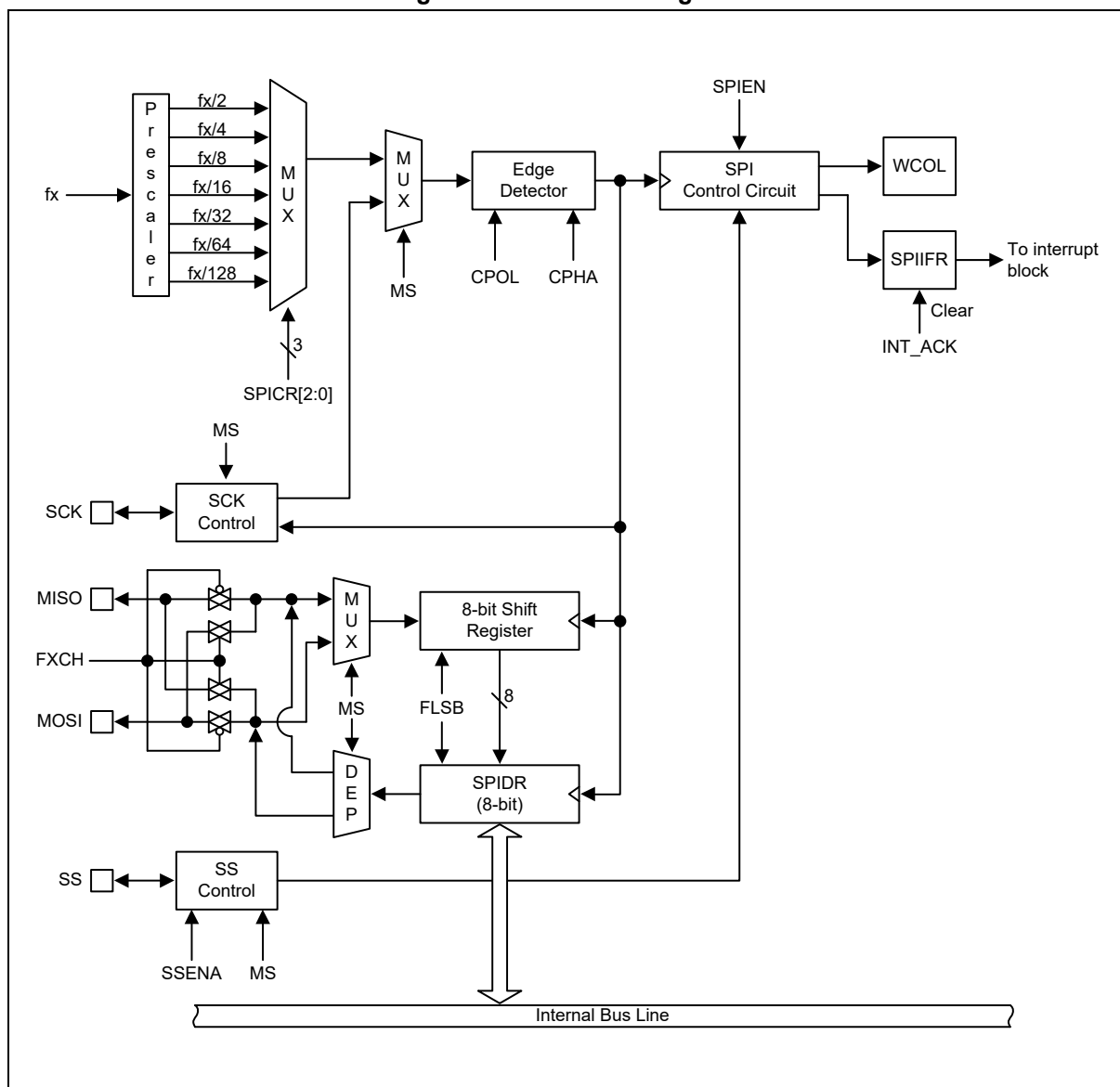
1. AN0~AN14 Function can be controlled by P0FSR, P1FSRL, and P1FSRH.
2. The pull-up resistor of P0/P1 can be enabled by P0PU/P1PU register. So, be careful of each P0/P1 pull-up resistor. If a pull-up resistor of P0/P1 is enabled, the corresponding pin will be changed to the equivalent resistor value by it.
3. An ADC wake-up interrupt can occur by a falling edge(VIL) of selected ANn pins.
4. ADC path is off when it is power-down mode and ADC wake-up interrupt path is on during power-down mode when ANnWEN bit is '1'.
5. n = 0, 1, 2, 3, ... and 14

17. SPI

There is serial peripheral interface (SPI) one channel in MC96F8316P. The SPI allows synchronous serial data transfer between the external serial devices. It can do Full-duplex communication by 4-wire (MOSI, MISO, SCK, SS), support master/slave mode, can select serial clock (SCK) polarity, phase and whether LSB first data transfer or MSB first data transfer.

17.1 SPI Block Diagram

Figure 30. SPI Block Diagram



18. UART 0/1

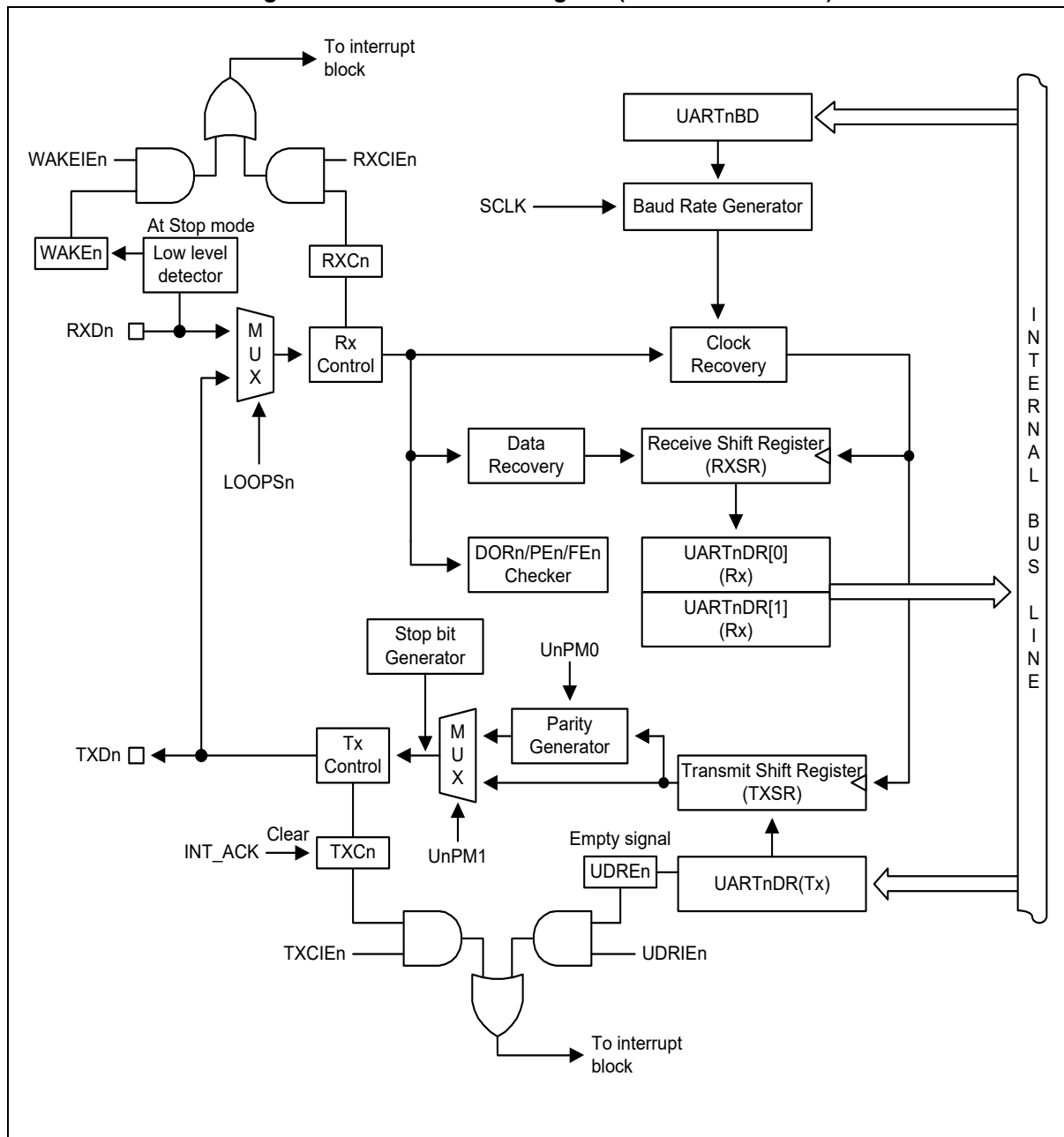
The MC96F8316P has built-in 2-channel of UART module (Universal Asynchronous Receiver/Transmitter).

The UART 0/1 of the MC96F8316P features the followings:

- Full-duplex and half-duplex operations
- Baud rate generator
- Supports serial frames with 5,6,7, or 8 Data bits and 1 or 2 Stop bits
- Odd or even parity generation, and parity check supported by hardware
- Data OverRun Detection
- Framing Error Detection
- Double Speed Asynchronous Communication Mode

18.1 UARTn Block Diagram

Figure 31. UARTn Block Diagram (Where n = 0 and 1)



19. Flash CRC and Checksum Generator

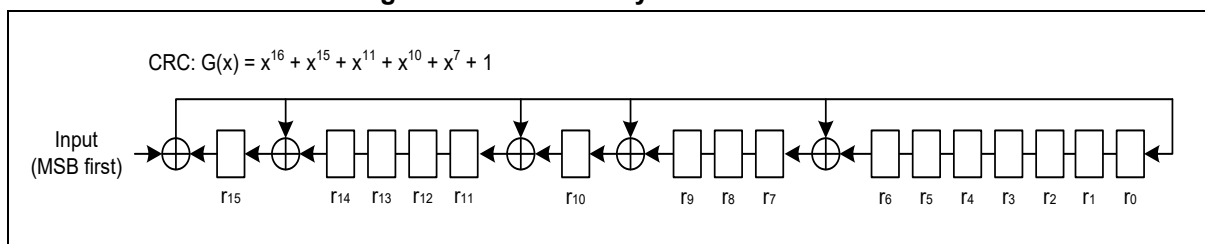
Flash CRC (Cyclic Redundancy Check) generator of MC96F8316P generates 16-bit CRC code bits from Flash and a generator polynomial. The CRC code for each input data frame is appended to the frame.

Specifically, CRC-based technique is used to verify data transmission or storage integrity. In the scope of the functional safety standards, this technique offers a means of verifying the Flash memory integrity. The Flash CRC generator helps compute a signature of software during runtime, to be compared with a reference signature.

The CRC generator has the following features:

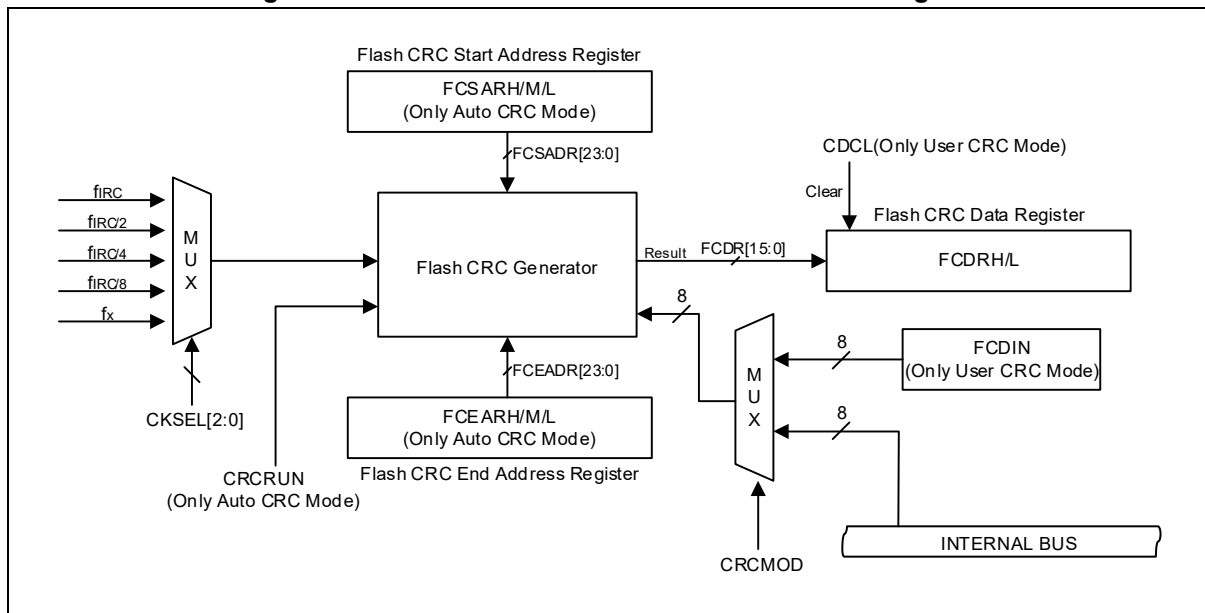
- Auto CRC and User CRC Mode
- CRC Clock : f_{IRC} , $f_{IRC}/2$, $f_{IRC}/4$, $f_{IRC}/8$ and f_x (System clock)
- CRC-16 polynomial: $0x8C81$ ($X^{16} + X^{15} + X^{11} + X^{10} + X^7 + 1$)

Figure 32. CRC-16 Polynomial Structure



19.1 Flash CRC and Checksum Generator Block Diagram

Figure 33. Flash CRC/Checksum Generator Block Diagram



20. Power Down Operation

MC96F8316P offers two power-down modes to minimize power consumption of itself. Programs under the two power saving modes IDLE and STOP, are stopped and power consumption is reduced considerably.

20.1 Peripheral Operation in IDLE/STOP Mode

Peripheral's operations during IDLE/STOP mode are described in Table 14.

Table 14. Peripheral Operation During Power-down Mode

Peripheral	IDLE Mode	STOP Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain
Basic Interval Timer	Operates Continuously	Stop
Watchdog Timer	Operates Continuously	Stop (Can be operated with WDTRC OSC)
Watch Timer	Operates Continuously	Stop (Can be operated with sub clock)
Timer0~2	Operates Continuously	Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally)
ADC	Operates Continuously	Stop
BUZ	Operates Continuously	Stop
SPI	Operates Continuously	Only operate with external clock
UART	Operates Continuously	Stop
I2C	Operates Continuously	Only operate with external clock
Internal OSC (16MHz)	Oscillation	Stop when the system clock (fx) is f _{IRC}
WDTRC OSC (5kHz)	Can be operated with setting value	Can be operated with setting value
Main OSC (0.4~12MHz)	Oscillation	Stop when $f_x = f_{XIN}$
Sub OSC (32.768kHz)	Oscillation	Stop when $f_x = f_{SUB}$
I/O Port	Retain	Retain
Control Register	Retain	Retain
Address Data Bus	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET, Timer Interrupt (EC0, EC1, EC2), SPI (External clock), External Interrupt, UART by RX, WT (sub clock), WDT, ADC

21. Reset

When a reset event occurs, an internal register is selected to be initialized in accordance with a reset value. Each reset value described in Table 15 indicates a corresponding on-chip Hardware that is to be initialized.

Table 15. Reset Value and Relevant On-chip Hardware

On-chip Hardware	Reset Value
Program Counter (PC)	0000H
Accumulator	00H
Stack Pointer (SP)	07H
Peripheral clock	On
Control register	Refer to peripheral registers.

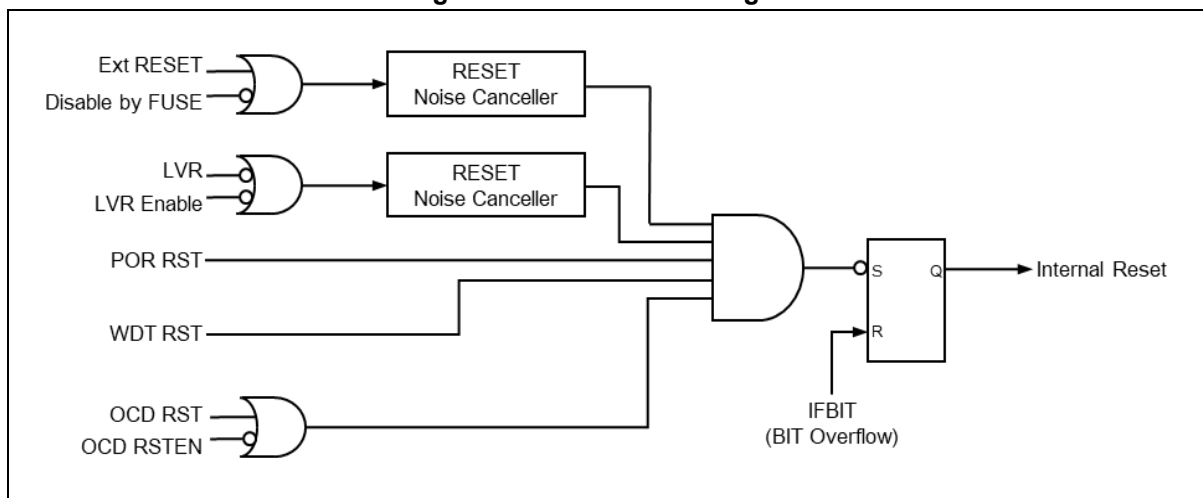
MC96F8316P has 5 types of reset sources as listed in the followings:

- External RESETB
- Power-on RESET (POR)
- WDT overflow reset (in a case of WDTEN='1')
- Low voltage reset (in a case of LVREN='0')
- OCD RESET

21.1 Reset Block Diagram

Figure 34 shows a reset block of MC96F8316P.

Figure 34. Reset Block Diagram



22. Flash Memory

MC96F8316P incorporates Flash memory inside. Program can be written, erased, and overwritten on Flash memory while it is mounted on a board. The Flash memory can be read by 'MOVC' instruction and programmed in OCD, serial ISP mode or user program mode.

Main features of the Flash memory are listed below:

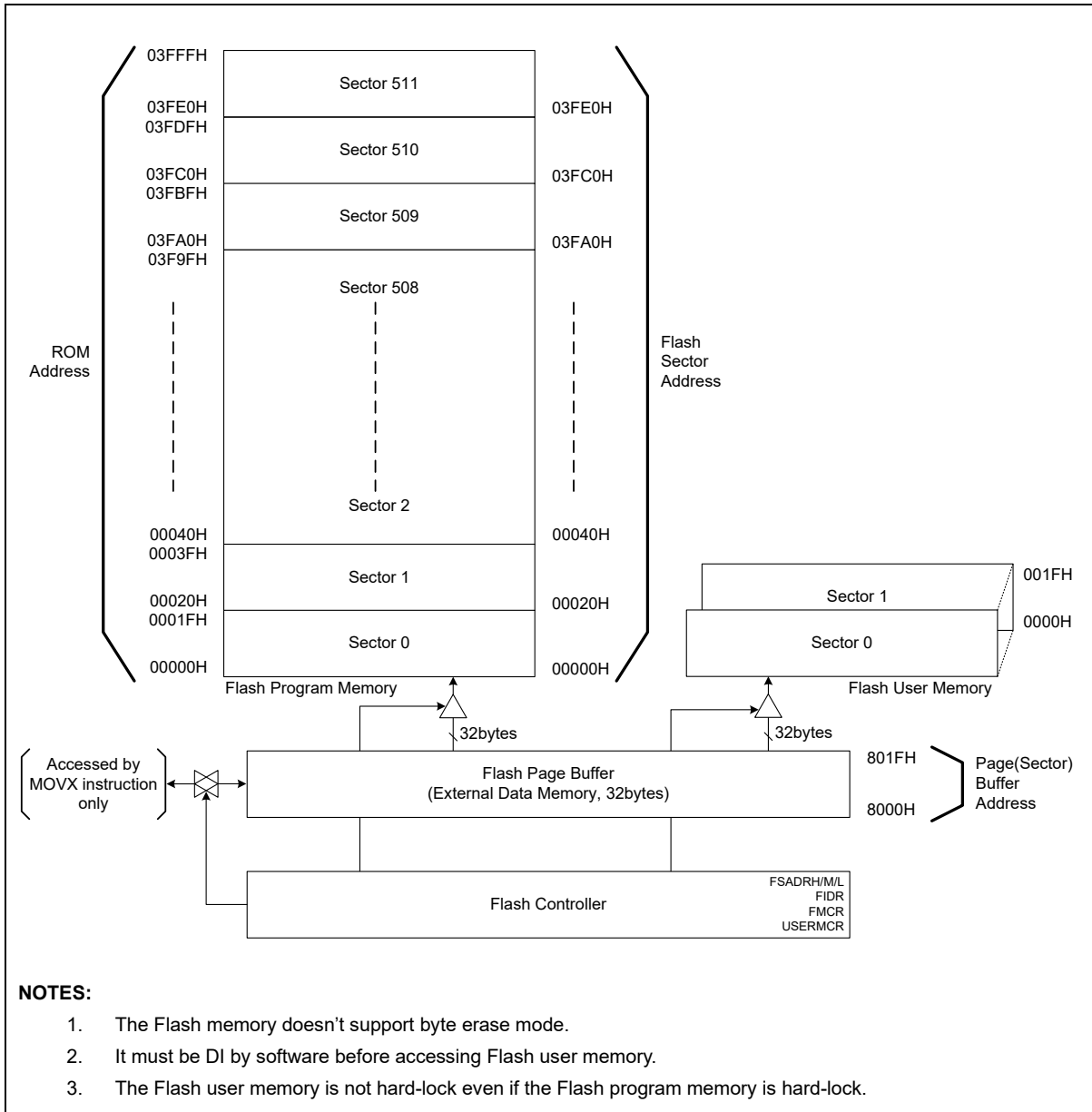
- Flash Size: 16 Kbytes
- Single power supply program and erase
- Command interface for fast program and erase operation
- Minimum 10,000 (Sector 0~503)/100,000 (504~511) program/erase cycles at typical voltage and temperature for Flash memory

NOTE:

1. It must be DI by software before accessing Flash user memory.

22.1 Flash Program ROM Structure

Figure 35. Flash program ROM Structure



23. Electrical Characteristics

23.1 Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply voltage	V _{IN}	-0.3 ~ +6.5		–
Normal voltage Pin	V _I	-0.3 ~ V _{DD} +0.3	V	Voltage on any pin with respect to V _{SS}
	V _O	-0.3 ~ V _{DD} +0.3		
	I _{OH}	-25	mA	Maximum current output sourced by (I _{OH} per I/O pin)
	∑I _{OH}	-200		Maximum current (∑I _{OH})
	I _{OL}	180		Maximum current sunk by (I _{OL} per I/O pin)
	∑I _{OL}	200		Maximum current (∑I _{OL})
Total power dissipation	P _T	600	mW	–
Operating temperature	T _{OP}	-40 ~ +105	°C	–
Storage temperature	T _{STG}	-65 ~ +150		–

CAUTION:

- Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

23.2 Recommended Operating Conditions

Table 17. Recommended Operating Conditions

(T_A=-40°C to +105°C)

Parameter	Symbol	Conditions	Typ.	Max.	Unit	
Operating voltage	V _{DD}	f _x = 32 to 38 kHz		2.0	5.5	V
		f _x = 0.4 to 4.2 MHz	SX-tal	2.2	5.5	
		f _x = 0.4 to 8 MHz	X-tal	2.4	5.5	
		f _x = 0.4 to 12 MHz		2.7	5.5	
		f _x = 0.5 to 16 MHz	Internal RC	1.8	5.5	
Operating temperature	T _{OPR}	V _{DD} = 1.8 to 5.5 V	-40	105	°C	

23.3 ADC Characteristics

Table 18. ADC Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Resolution	–	–	–	12	–	bit	
Integral Non-linearity	INL	VDD = 2.7 to 5.5 V, f _x = 8 MHz	–	–	±6	LSB	
Differential Non-linearity	DNL		–	–	±1		
Top offset error	TOE		–	–	±5		
Zero offset error	ZOE		–	–	±5		
Conversion time	t _{CON}	VDD = 4.0 to 5.5 V	20	–	–	μs	
		VDD = 3.0 to 5.5 V	30	–	–		
		VDD = 2.7 to 5.5 V	60	–	–		
Analog input voltage	V _{AN}	–	V _{SS}	–	AVREF	V	
Analog reference voltage	AVREF	⁽³⁾	1.8	–	VDD		
VDD15	–	–	–	1.55	–		
A/DC input leakage current	I _{AN}	VDD = 5.12 V	–	–	2	μA	
A/DC current	I _{ADC}	Enable	–	–	1	2	mA
		Disable		–	–	0.1	μA

NOTES:

1. Zero offset error is the difference between 000000000 and the converted output for zero input voltage (V_{SS}).
2. The top offset error is the difference between 111111111 and the converted output for top input voltage (VDD).
3. If AVREF is less than 2.7 V, the resolution degrades by 1-bit whenever AVREF drops 0.1 V. (@ADCLK = 0.5 MHz, under 2.7 V resolution has no test.)

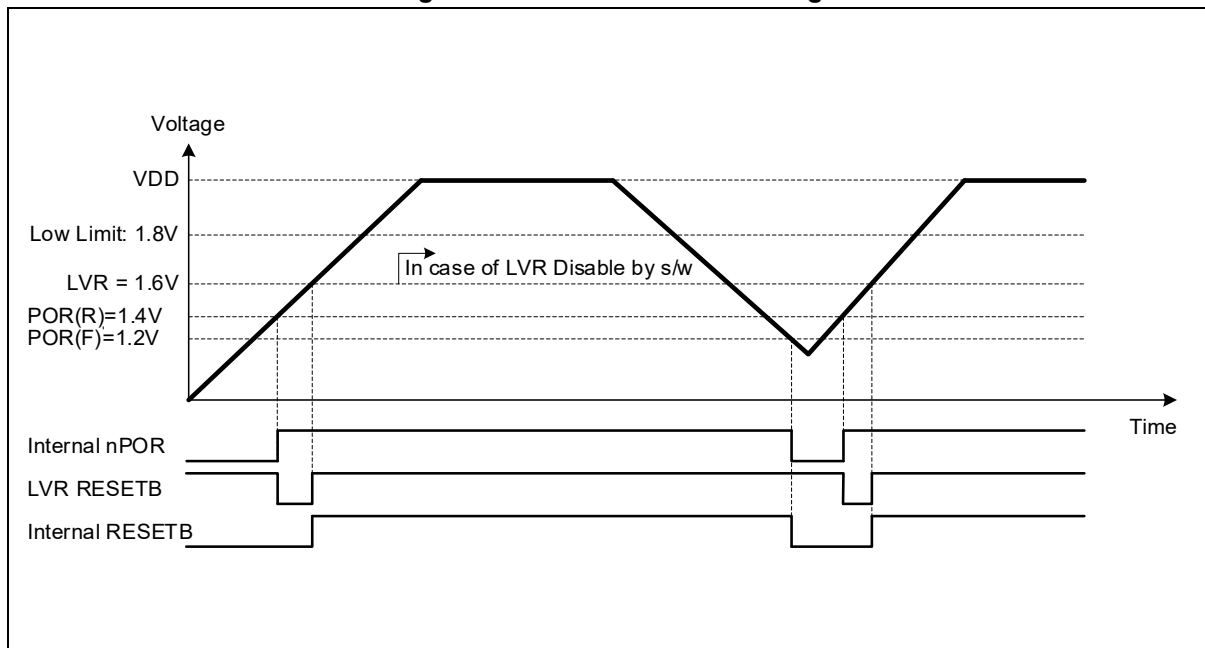
23.4 Power-on Reset

Table 19. Power-on Reset Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESET release level	V_{POR}	–	–	1.4	–	V
Hysteresis	ΔV	–	–	0.1	–	
VDD Voltage Rising Time	t_R	0.5 V – 2 V	0.05	–	100	V/ms
POR current	I_{POR}	–	–	0.2	–	μA

Figure 36. Power-on Reset Timing



23.5 Low Voltage Reset and Low Voltage Indicator Characteristics

Table 20. LVR and LVI Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Detection level	VLVR VLVI	<ul style="list-style-type: none"> • LVR: All levels • LVI: other levels except 1.60 V • 1.60V level: Rising edge voltage • Other levels: Falling edge voltage 		–	1.60	1.79	V
				1.84	2.00	2.16	
				1.93	2.10	2.27	
				2.02	2.20	2.38	
				2.13	2.32	2.51	
				2.24	2.44	2.64	
				2.38	2.59	2.80	
				2.53	2.75	2.97	
				2.70	2.93	3.16	
				2.89	3.14	3.39	
				3.11	3.38	3.65	
				3.37	3.67	3.97	
				3.68	4.00	4.32	
4.06	4.40	4.74					
LVR/LVI Hysteresis	ΔV	–		–	100	180	mV
Minimum pulse width	t_{LW}	–		100	–	–	μs
LVR and LVI current	I_{BL}	Enable	$V_{DD} = 3\text{ V}$	–	10.0	18.0	μA
		Disable	$V_{DD} = 3\text{ V}$	–	–	0.1	

23.6 Internal RC Oscillator Characteristics

Table 21. Internal RC Oscillator Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{IRC}	$V_{DD} = 1.8\text{ V}$ to 5.5 V	–	16	–	MHz
Tolerance	–	$T_A = -20^\circ\text{C}$ to $+70^\circ\text{C}$ (User trim, Using only E-PGM+)	–	–	± 1.0	%
		$T_A = -20^\circ\text{C}$ to $+70^\circ\text{C}$	–		± 1.5	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	–		± 2.0	
		$T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$	–		± 3.0	
Clock duty ratio	T_{OD}	–	40	50	60	%
Stabilization time	t_{HFS}	–	–	–	100	μs
Internal RC Current	I_{IRC}	Enable	–	0.6	–	mA
		Disable	–	–	0.1	μA

NOTES:

1. User Trimming means the calibration of IRC frequency. Using E-PGM+.
2. To ensure $\pm 1.0\%$ tolerance of IRC frequency, it is necessary to do User Trimming.
3. Guaranteed by design but might be On-board programming after SMT process.
(IRC Calibration with high temperature can cause the shift of the frequency, be sure to calibrate enough to cool to near room temperature after SMT process)

23.7 Internal Watchdog Timer RC Oscillator Characteristics

Table 22. Internal WDTRC Oscillator Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization time	t_{WDTS}	–	–	–	1	ms
WDTRC current	I_{WDTRC}	Enable	–	1	–	μA
		Disable	–	–	0.1	

23.8 DC Characteristics

Table 23. DC Characteristics

(T_A=-40°C to +105°C, VDD=1.8 V to 5.5 V, VSS=0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input high voltage	V _{IH}	All input pins, RESETB		0.8VDD	–	VDD	V
Input low voltage	V _{IL}	All input pins, RESETB		–	–	0.2VDD	V
Output high voltage	V _{OH1}	VDD = 4.5 V, IOH = -20 mA, All output ports except V _{OH2}		VDD-2.0	–	–	V
	V _{OH2}	VDD = 4.5 V, IOH = -10 mA, P2[5:0]		VDD-2.0	–	–	V
Output low voltage	V _{OL1}	VDD = 4.5 V, IOL = 15 mA, All output ports except V _{OL2}		–	–	1.2	V
	V _{OL2}	VDD = 4.5 V, P2[5:0] and P1[7:6]	IOL = 160 mA; Up to 85°C	–	1.5	3.0	V
	IOL = 120 mA; Up to 105°C						
Input high leakage current	I _{IH}	All output ports		–	–	1.0	μA
Input low leakage current	I _{IL}	All output ports		-1.0	–	–	μA
Pull-up resistor	R _{PU1}	VI=0 V, T _A =25°C, All Input ports	VDD = 5 V	25	50	100	kΩ
			VDD = 3 V	50	100	200	
	R _{PU2}	VI=0 V, T _A =25°C, RESETB	VDD = 5 V	150	250	400	
			VDD = 3 V	300	500	700	
ADC wake-up Pull-up resistor	R _{AWPU1}	T _A =25°C		90	150	200	kΩ
	R _{AWPU2}			180	300	400	
OSC feedback resistor	R _{X1}	XIN = VDD, XOUT = VSS T _A =25°C, VDD = 5 V		600	1200	2000	kΩ
	R _{X2}	SXIN = VDD, SXOUT = VSS T _A =25°C, VDD = 5 V		2500	5000	10000	kΩ

23.9 Supply Current Characteristics

Table 24. Supply Current Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V , $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current	I _{DD1} (RUN)	f _{XIN} = 12 MHz, VDD = 5 V±10%	–	2.5	5.0	mA
		f _{XIN} = 10 MHz, VDD = 3 V±10%	–	1.8	3.6	
		f _{IRC} = 16 MHz, VDD = 5 V±10%	–	2.0	4.0	
	I _{DD2} (IDLE)	f _{XIN} = 12 MHz, VDD = 5 V±10%	–	1.5	3.0	mA
		f _{XIN} = 10 MHz, VDD = 3 V±10%	–	0.7	1.4	
		f _{IRC} = 16 MHz, VDD = 5 V±10%	–	1.0	2.0	
	I _{DD3} (RUN)	f _{SUB} = 32.768 kHz, VDD = 3 V±10%, T _A = 25°C	–	170	270	µA
	I _{DD4} (IDLE)	f _{SUB} = 32.768 kHz, VDD = 3V±10%, T _A = 25°C	–	6.0	12.0	µA
	I _{DD5} (STOP)	VDD = 5 V±10%, T _A = 25°C	–	1.5	5.0	µA

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub oscillator. The IRC is an internal RC oscillator, and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the Power-on Reset (POR) block.

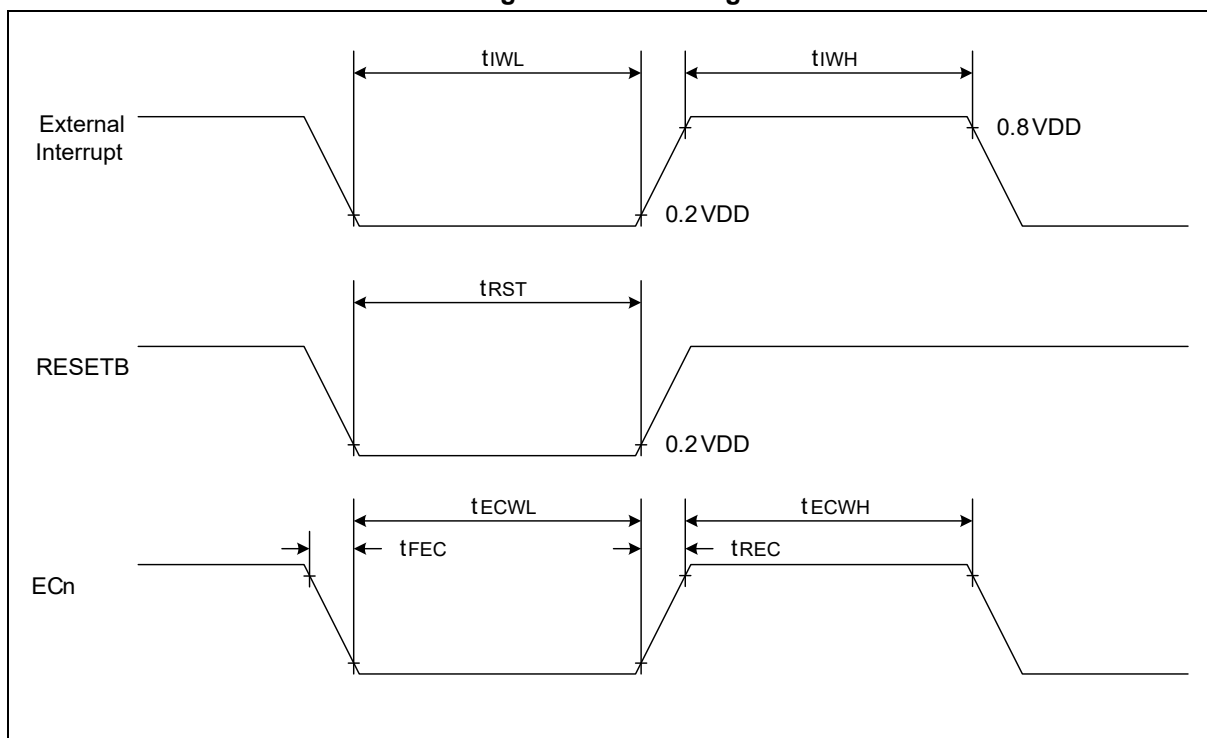
23.10 AC Characteristics

Table 25. AC Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RESETB input low width	t_{RST}	$V_{DD} = 5\text{ V}$	10	–	–	μs
Interrupt input high, low width	t_{IWH} , t_{IWL}	All interrupt, $V_{DD} = 5\text{ V}$	200	–	–	ns
External counter input high, low pulse width	t_{ECWH} , t_{ECWL}	EC_n , $V_{DD} = 5\text{ V}$ ($n=0, 1, 2$)	200	–	–	
External counter transition time	t_{REC} , t_{FEC}	EC_n , $V_{DD} = 5\text{ V}$ ($n=0, 1, 2$)	20	–	–	

Figure 37. AC Timing



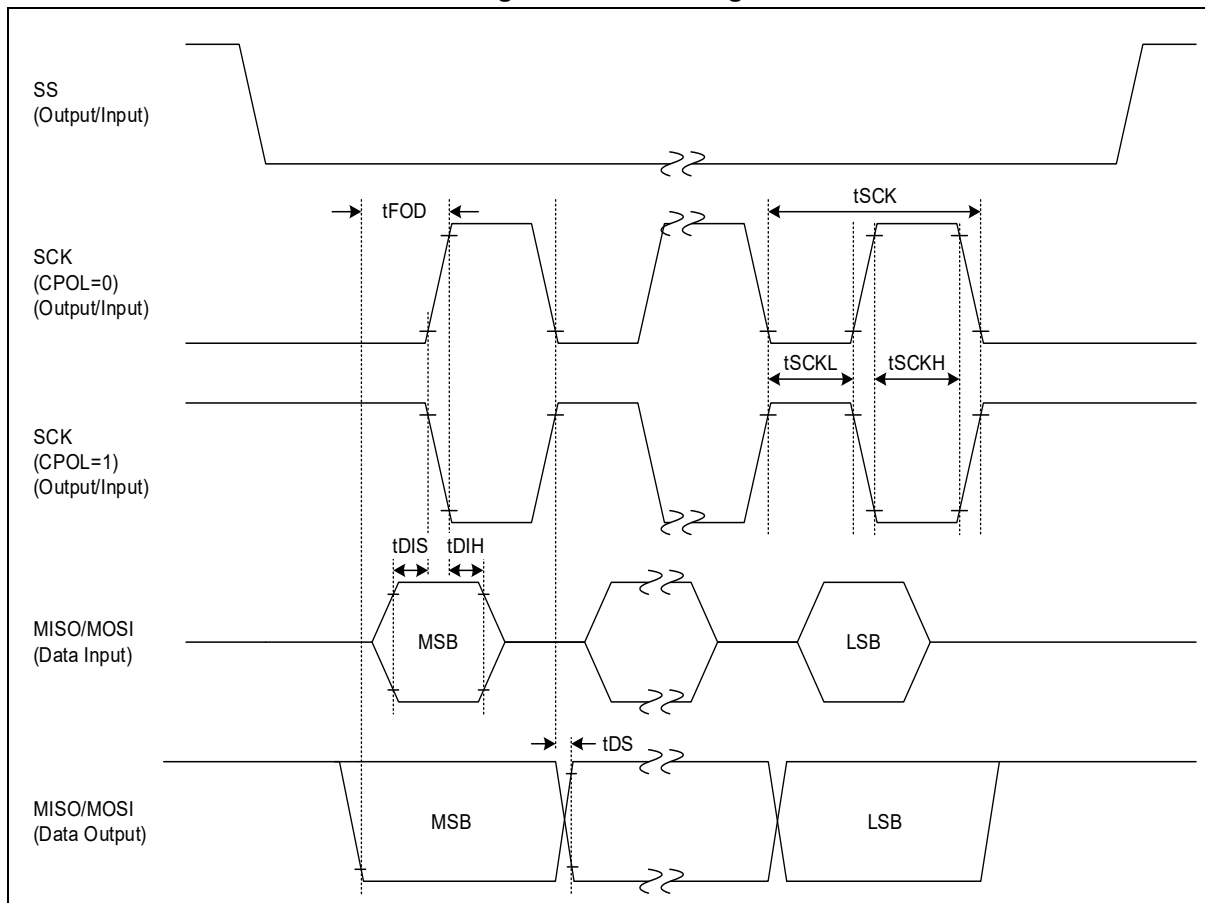
23.11 SPI Characteristics

Table 26. SPI Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output clock pulse period	t_{SCK}	Internal SCK source	1000	–	–	ns
Input clock pulse period		External SCK source	1000	–	–	
Output clock high, low pulse width	t_{SCKH}	Internal SCK source	350	–	–	
Input clock high, low pulse width	t_{SCKL}	External SCK source	350	–	–	
First output clock delay time	t_{FOD}	Internal/external SCK source	500	–	–	
Output clock delay time	t_{DS}	–	–	–	250	
Input setup time	t_{DIS}	–	500	–	–	
Input hold time	t_{DIH}	–	750	–	–	

Figure 38. SPI Timing



23.12 UART Timing Characteristics

Table 27. UART Timing Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 2.2\text{ V}$ to 5.5 V , $f_x = 11.1\text{ MHz}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial port clock cycle time	t_{SCK}	1250	$t_{CPU} \times 16$	1650	ns
Output data setup to clock rising edge	t_{S1}	590	$t_{CPU} \times 13$	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	$t_{CPU} - 50$	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	$t_{CPU} \times 8$	970	

Figure 39. UART Timing Characteristics

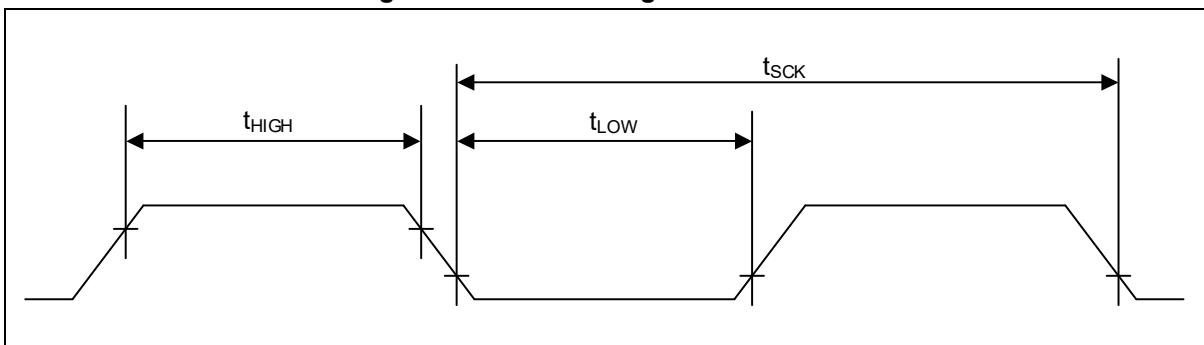
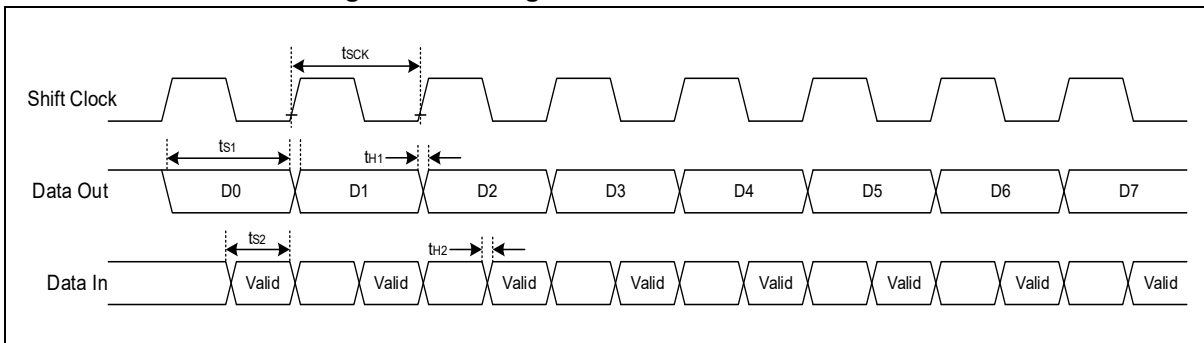


Figure 40. Timing Waveform of UART Module



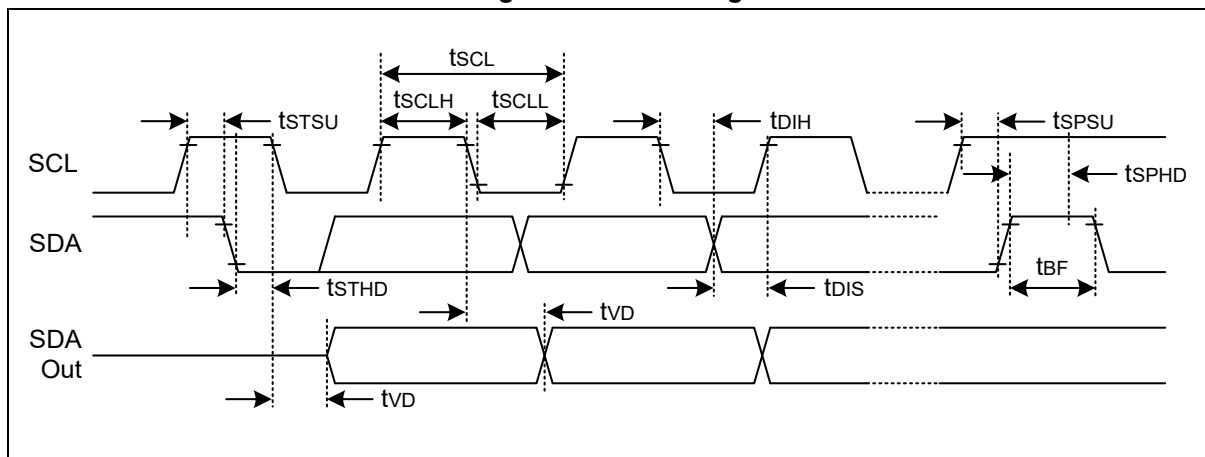
23.13 I2C Characteristics

Table 28. I2C Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		Min.	Max.	Min.	Max.	
Clock frequency	tSCL	0	100	0	400	kHz
Clock High Pulse Width	tSCLH	4.0	–	0.6	–	
Clock Low Pulse Width	tSCLL	4.7	–	1.3	–	
Bus Free Time	tBF	4.7	–	1.3	–	
Start Condition Setup Time	tSTSU	4.7	–	0.6	–	
Start Condition Hold Time	tSTHD	4.0	–	0.6	–	
Stop Condition Setup Time	tSPSU	4.0	–	0.6	–	
Stop Condition Hold Time	tSPHD	4.0	–	0.6	–	
Output Valid from Clock	tVD	0	–	0	–	
Data Input Hold Time	tDIH	0	–	0	1.0	
Data Input Setup Time	tDIS	250	–	100	–	
						ns

Figure 41. I2C Timing



23.14 Data Retention Voltage in STOP Mode

Table 29. Data Retention Voltage in STOP Mode

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	$V_{DDDR} = 1.8\text{ V}$ ($T_A = 25^\circ\text{C}$), STOP mode	–	–	1	μA

Figure 42. STOP Mode Release Timing when Initiated by Interrupt

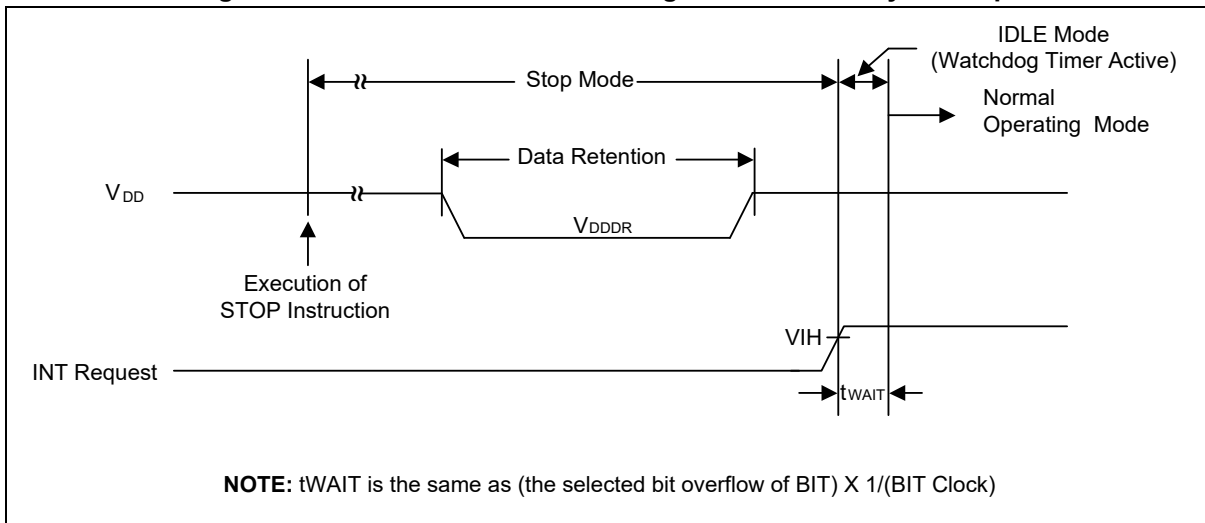
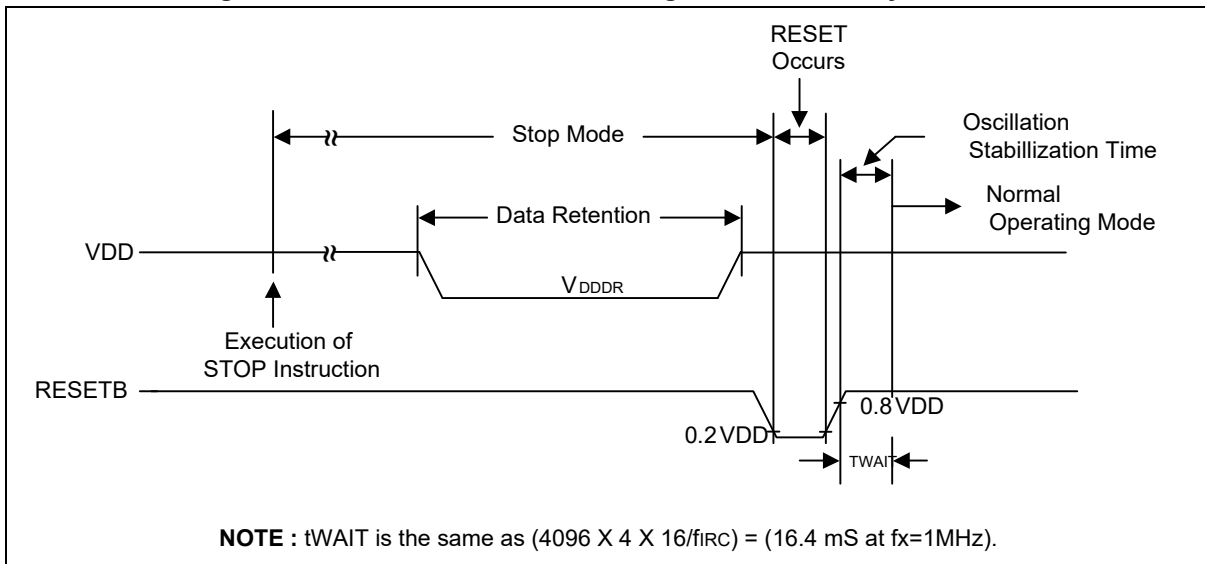


Figure 43. STOP Mode Release Timing when Initiated by RESETB



23.15 Internal Flash Characteristics

Table 30. Internal Flash Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sector write time	t_{FSW}	–	–	3.0	3.5	ms
Sector erase time	t_{FSE}	–	–	3.0	3.5	
Code write protection time	t_{FHL}	–	–	3.0	3.5	
Page buffer reset time	t_{FBR}	–	–	–	5	μs
System clock frequency	f_{SCLK}	–	0.4	–	–	MHz
Endurance of write/erase (Sector 0~503)	N_{FWE}	–	10,000	–	–	times
Endurance of write/erase (Sector 504~511)			100,000			
Flash Retention Time	t_{FRT}	–	10	–	–	years

23.16 Input/output Capacitance Characteristics

Table 31. I/O Capacitance Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	$f_x = 1\text{ MHz}$ Unmeasured pins are connected to VSS.	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

23.17 Main Oscillator Characteristics

Table 32. Main Oscillator Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 2.2\text{ V}$ to 5.5 V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal/ Ceramic Oscillator	Main oscillation frequency	2.2 V – 5.5 V	0.4	–	4.2	MHz
		2.4 V – 5.5 V	0.4	–	8.0	
		2.7 V – 5.5 V	0.4	–	12.0	
External Clock	XIN input frequency	2.2 V – 5.5 V	0.4	–	4.2	
		2.4 V – 5.5 V	0.4	–	8.0	
		2.7 V – 5.5 V	0.4	–	12.0	

Figure 44. Crystal/Ceramic Oscillator

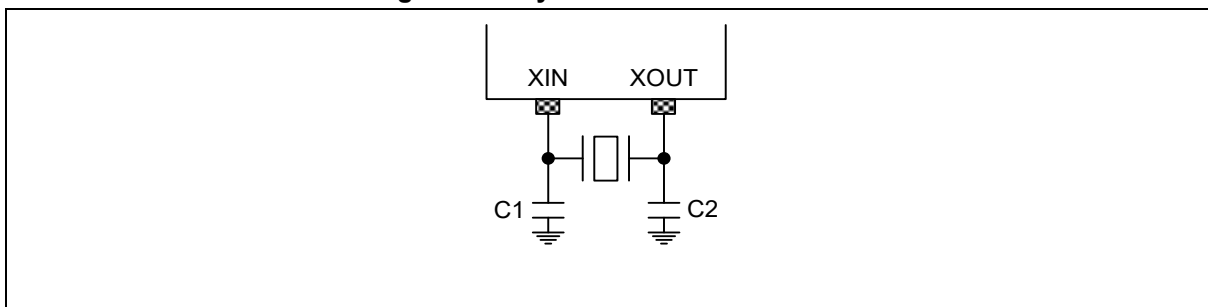
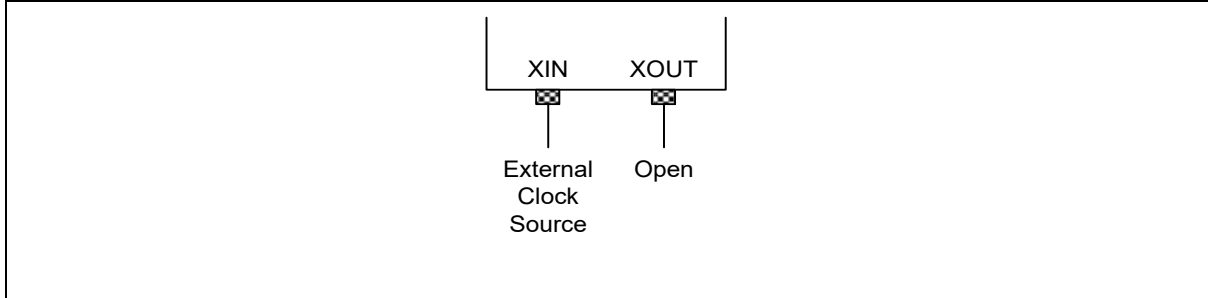


Figure 45. External Clock



23.18 Sub Oscillator Characteristics

Table 33. Sub Oscillator Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{DD} = 2.0\text{ V}$ to 5.5 V)

Oscillator	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal	Sub oscillation frequency	2.0 V – 5.5 V	32	32.768	38	kHz
External clock	SXIN input frequency		32	–	100	

Figure 46. Crystal Oscillator

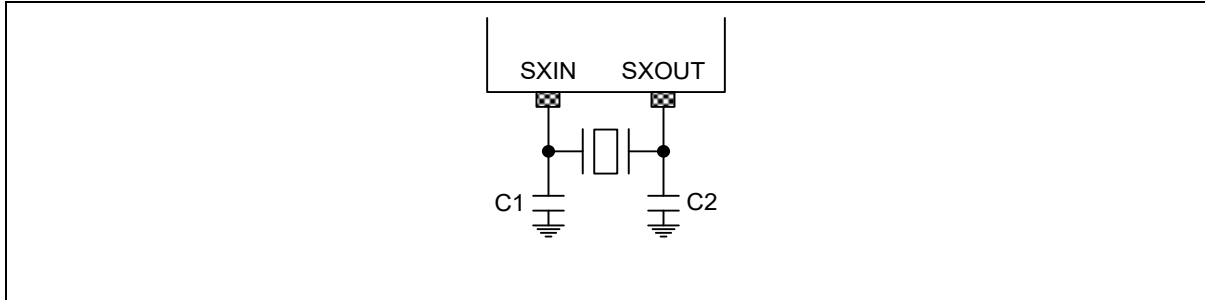
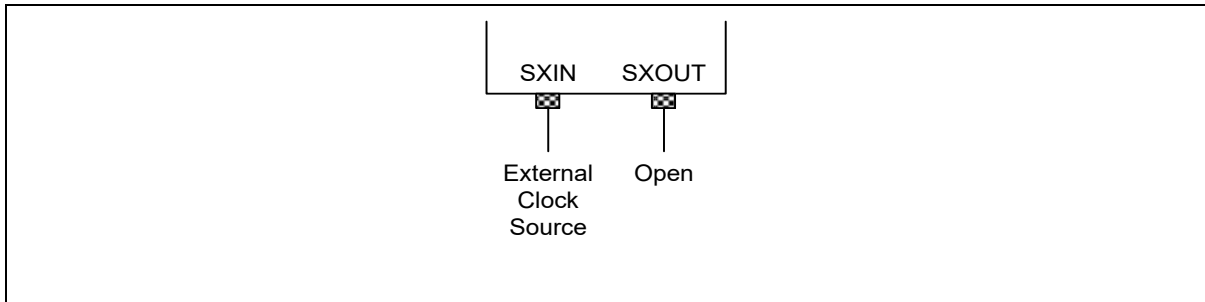


Figure 47. External Clock



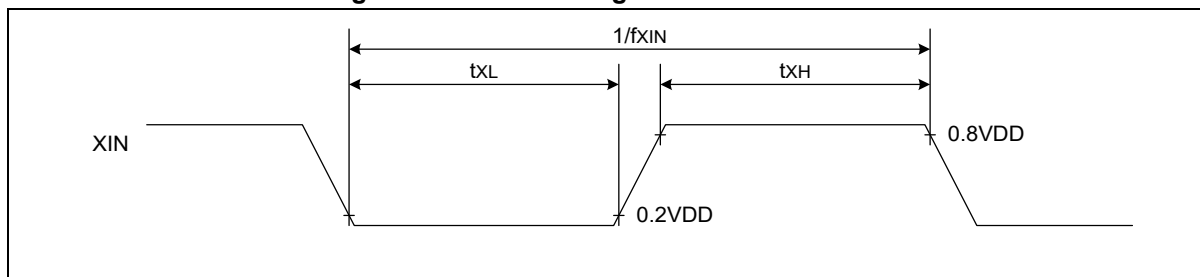
23.19 Main Oscillator Stabilization Characteristics

Table 34. Main Oscillator Stabilization Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 2.2\text{ V}$ to 5.5 V)

Oscillator	Conditions	Min.	Typ.	Max.	Unit
Crystal	$f_{XIN} \geq 1\text{ MHz}$ Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic		–	–	10	
External Clock	$f_{XIN} = 0.4$ to 12 MHz XIN input high and low width (t_{XL} , t_{XH})	42	–	1,250	ns

Figure 48. Clock Timing Measurement at XIN



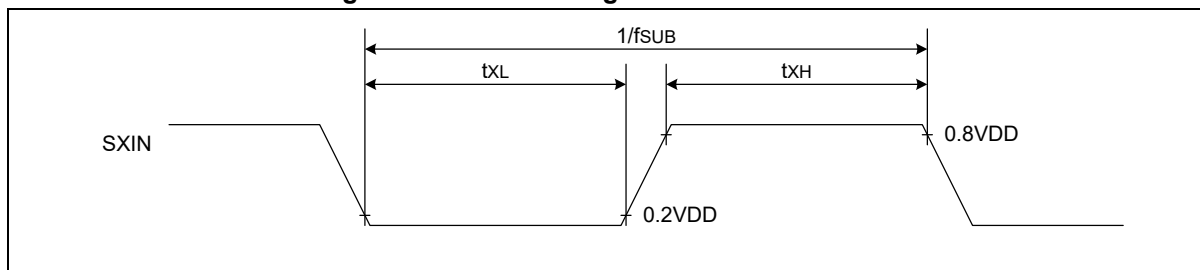
23.20 Sub Oscillator Stabilization Characteristics

Table 35. Sub Oscillator Stabilization Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{DD} = 2.0\text{ V}$ to 5.5 V)

Oscillator	Conditions	Min.	Typ.	Max.	Unit
Crystal	–	–	–	10	sec
	$V_{DD} = 3\text{ V}$, $T_A = 25^\circ\text{C}$	–	0.7	1.5	
External Clock	$SXIN$ input high and low width (t_{XL} , t_{XH})	5	–	15	us

Figure 49. Clock Timing Measurement at SXIN



23.21 Operating Voltage Range

Figure 50. Operating Voltage Range

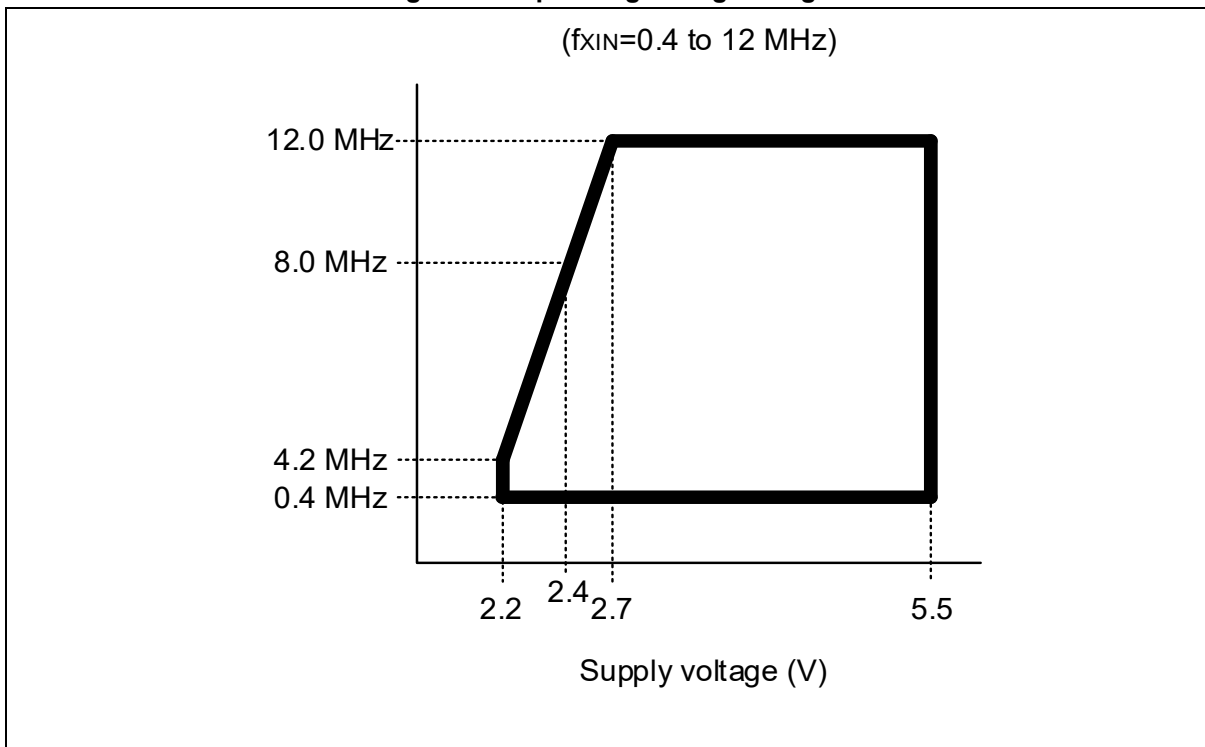
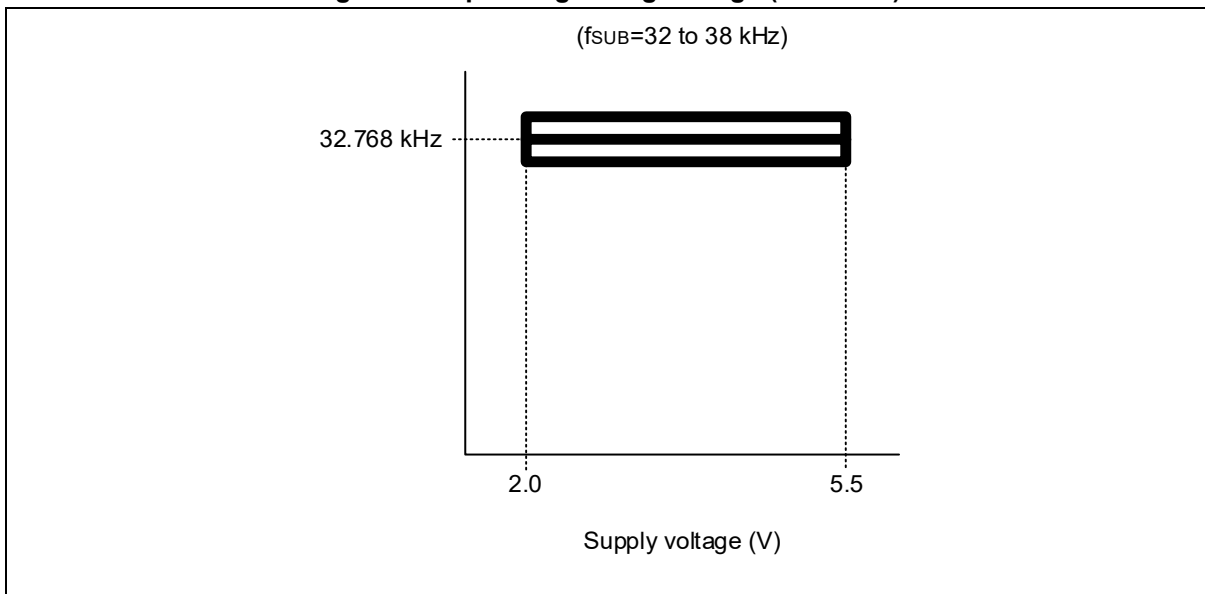


Figure 51. Operating Voltage Range (Sub OSC)



23.22 Typical Characteristics

Figures and tables described in this chapter can be used only for design guidance and are not tested or guaranteed. In graphs or tables some data may exceed the specified operating range and can be only for information. The device is guaranteed to operate properly only within the specified range.

The data presented in this chapter is a statistical summary of data collected on units from different lots over a period. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

Figure 52. MAIN RUN (IDD1) Current

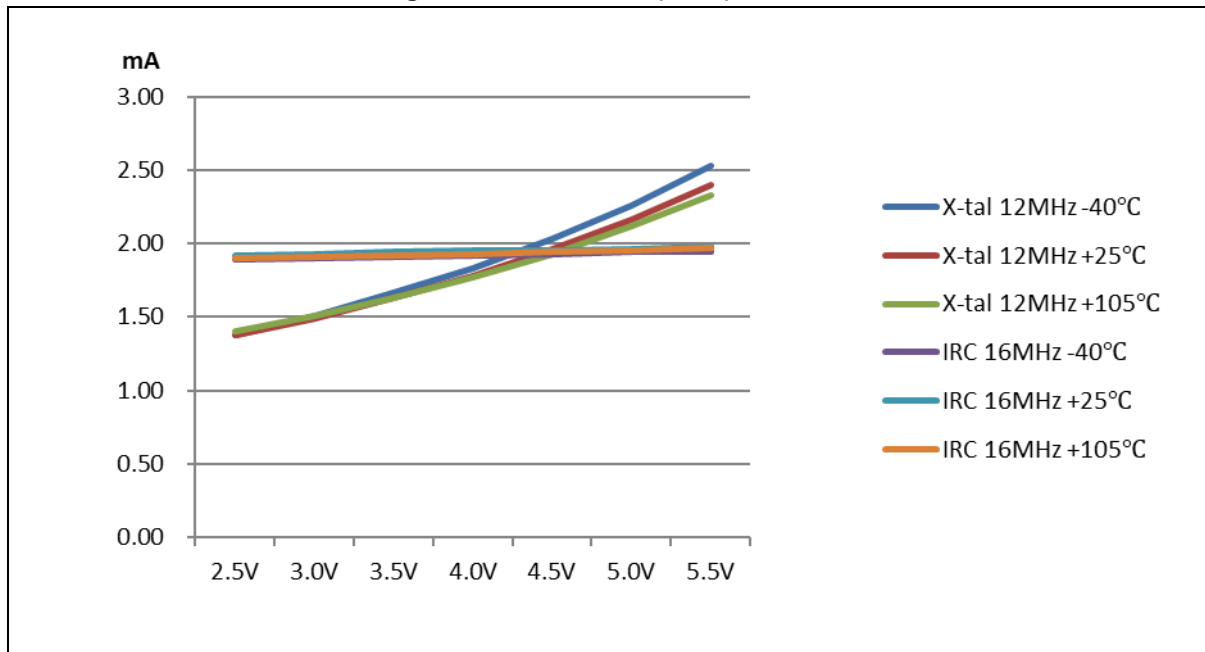


Figure 53. MAIN IDLE (IDD2) Current

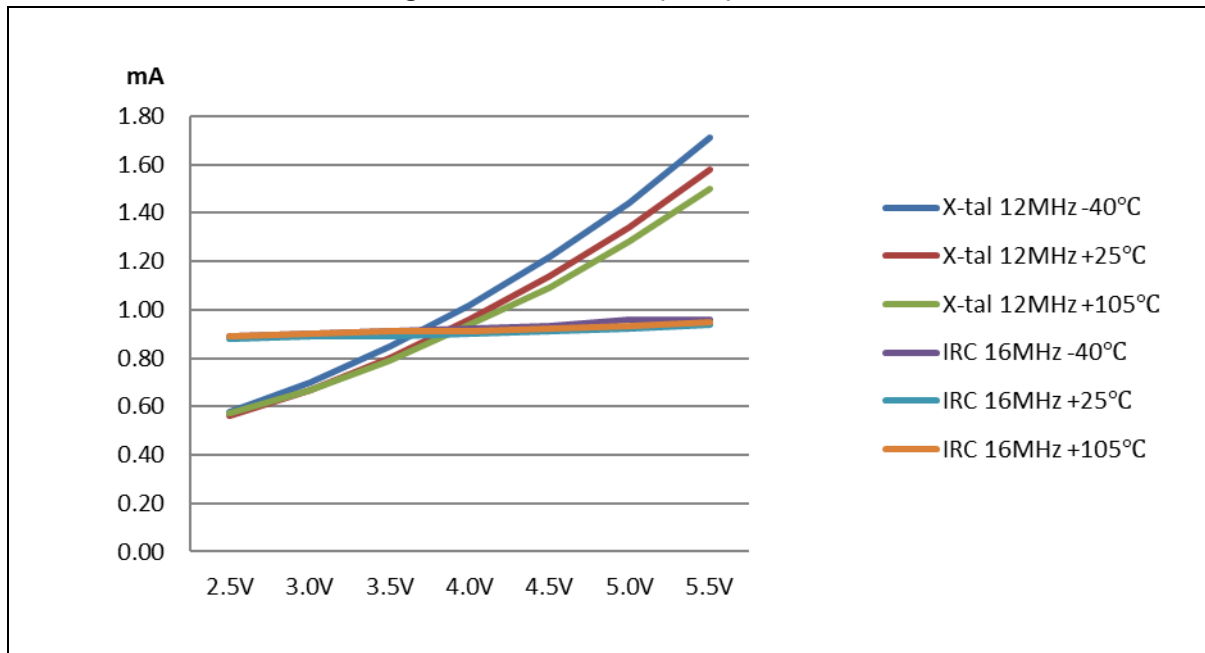


Figure 54. SUB RUN (IDD3) Current

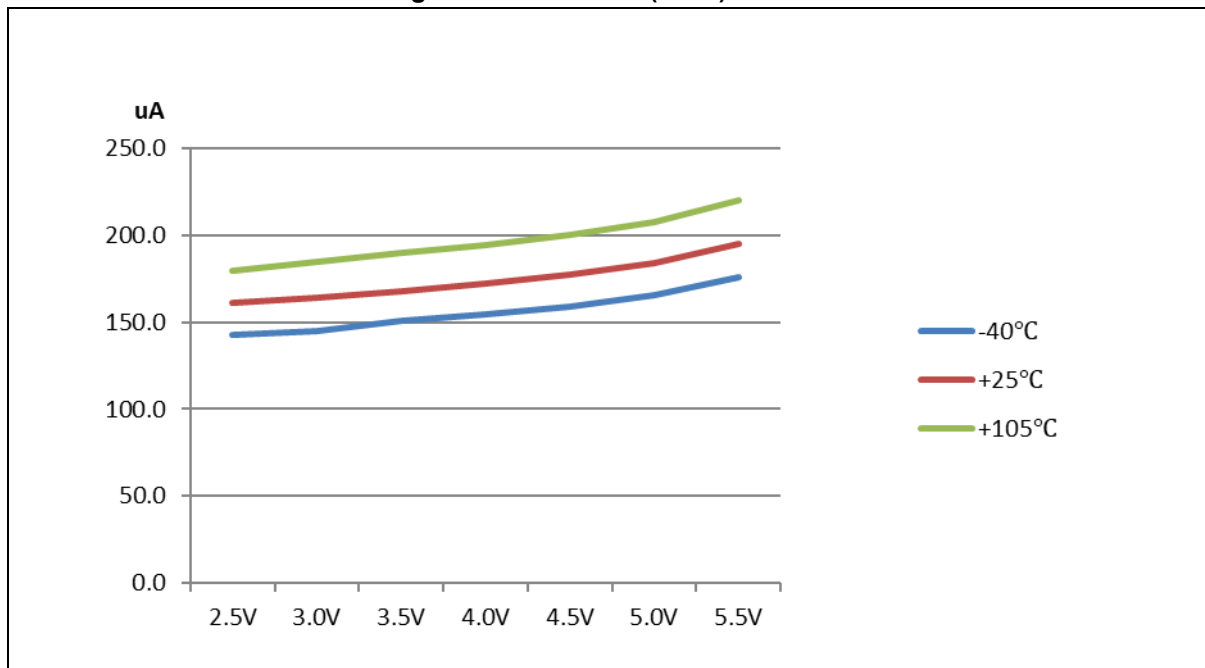


Figure 55. SUB IDLE (IDD4) Current

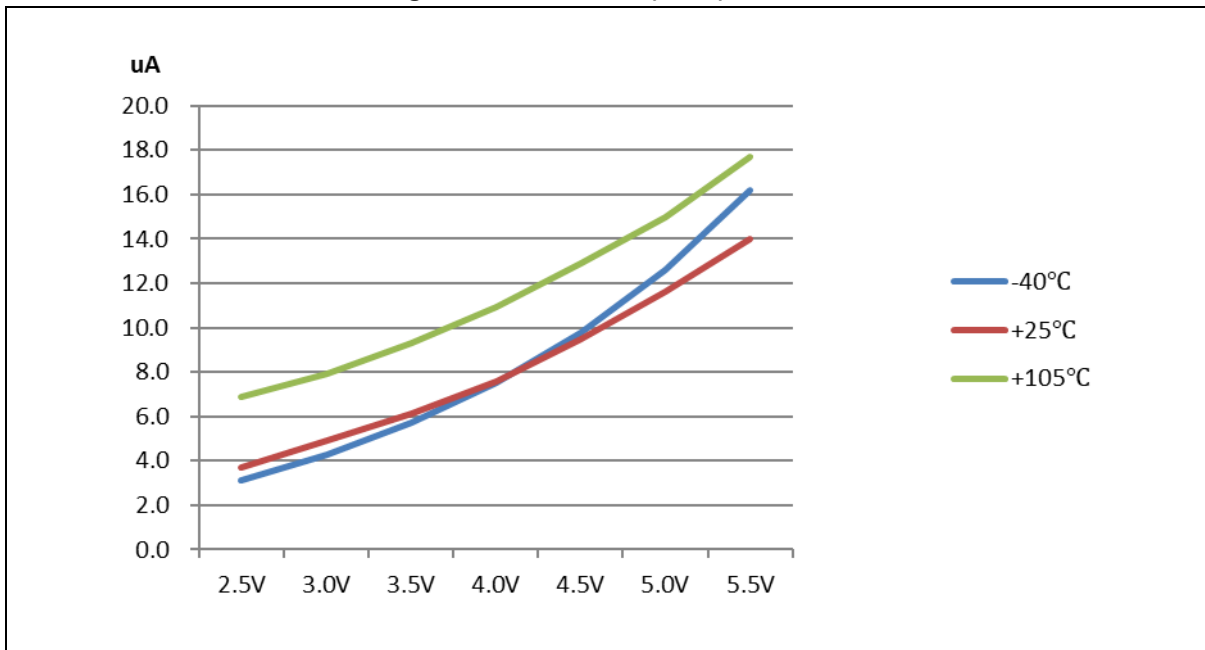
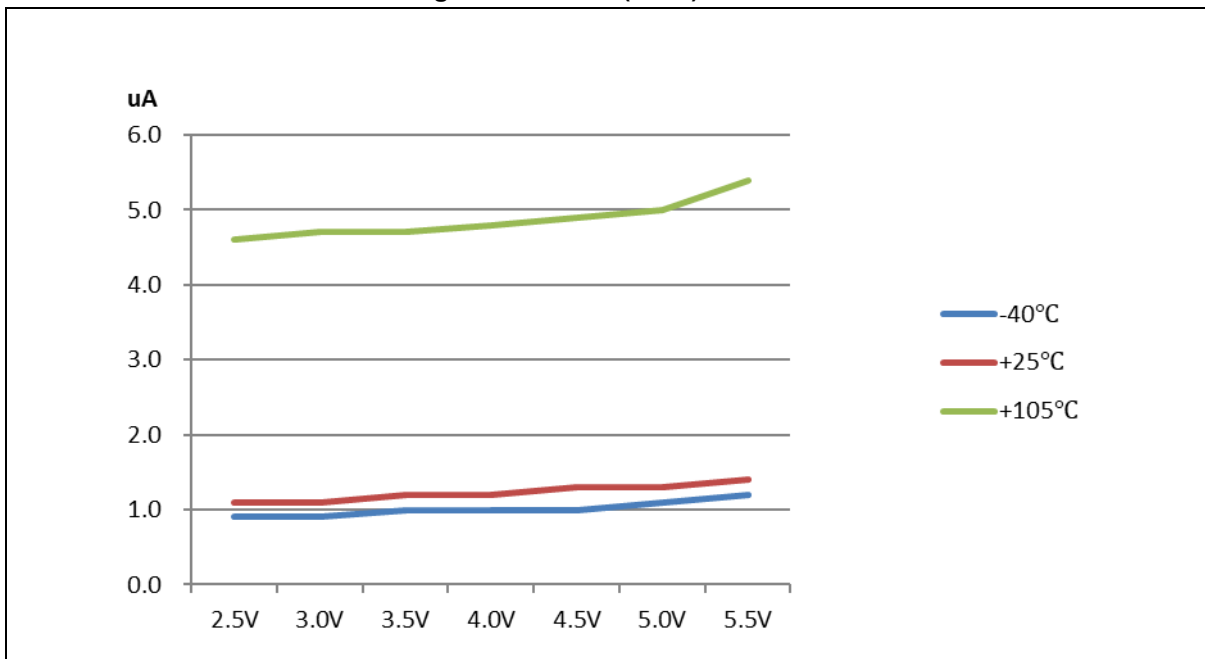


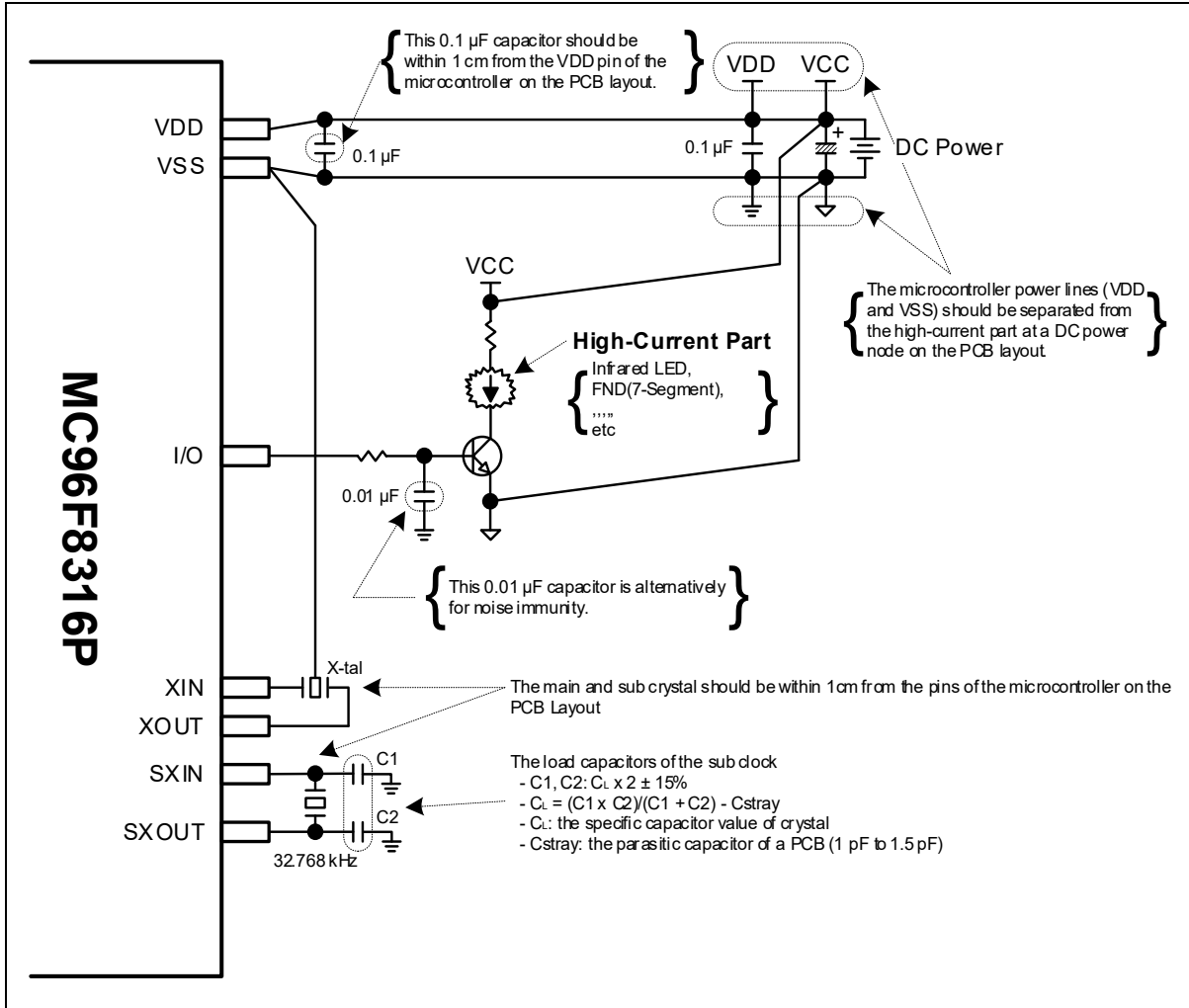
Figure 56. STOP (IDD5) Current



23.23 Recommended Circuit and Layout

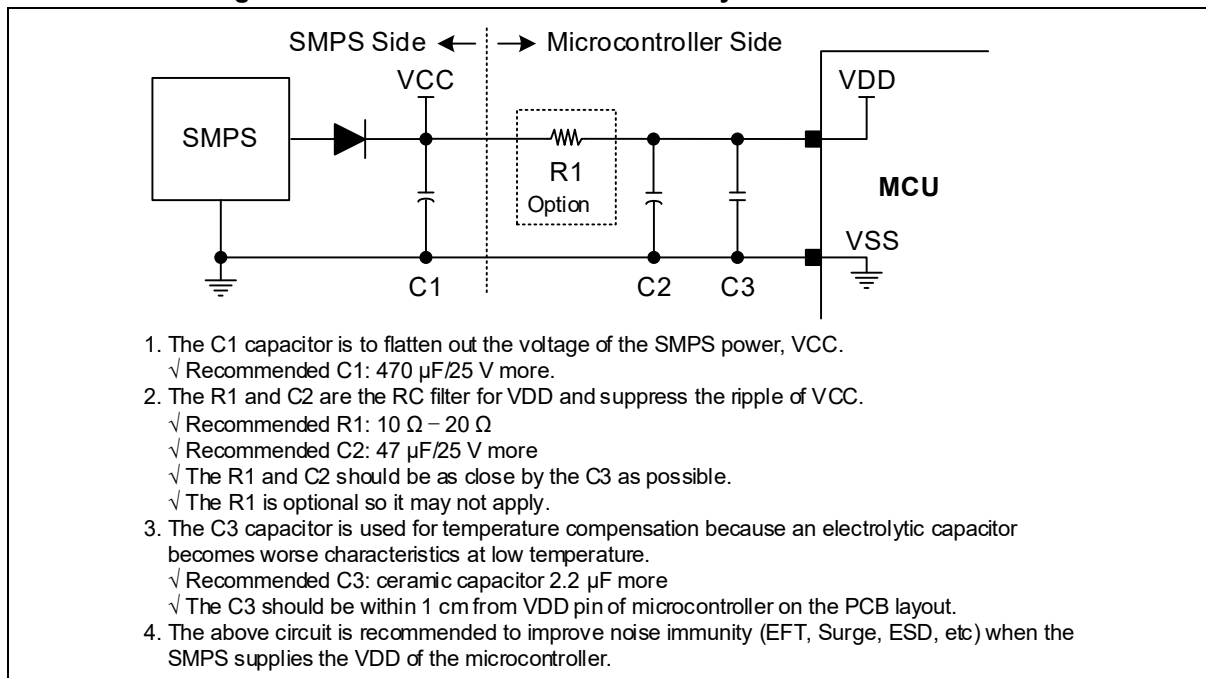
The Figure 57 is a recommended circuit and layout for MC96F8316P.

Figure 57. Recommended Circuit and Layout



23.24 Recommended Circuit and Layout with SMPS Power

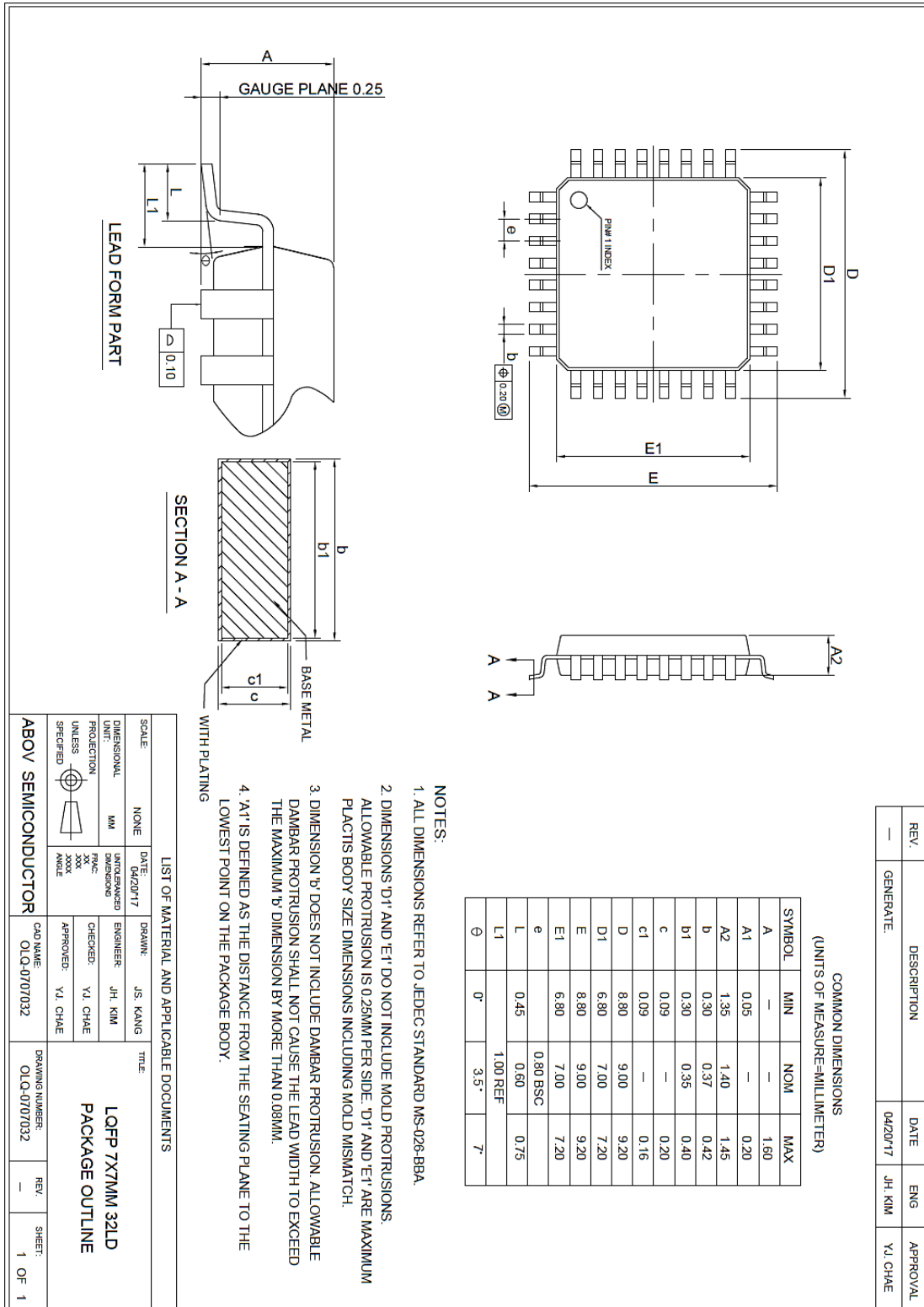
Figure 58. Recommended Circuit and Layout with SMPS Power



24. Package Information

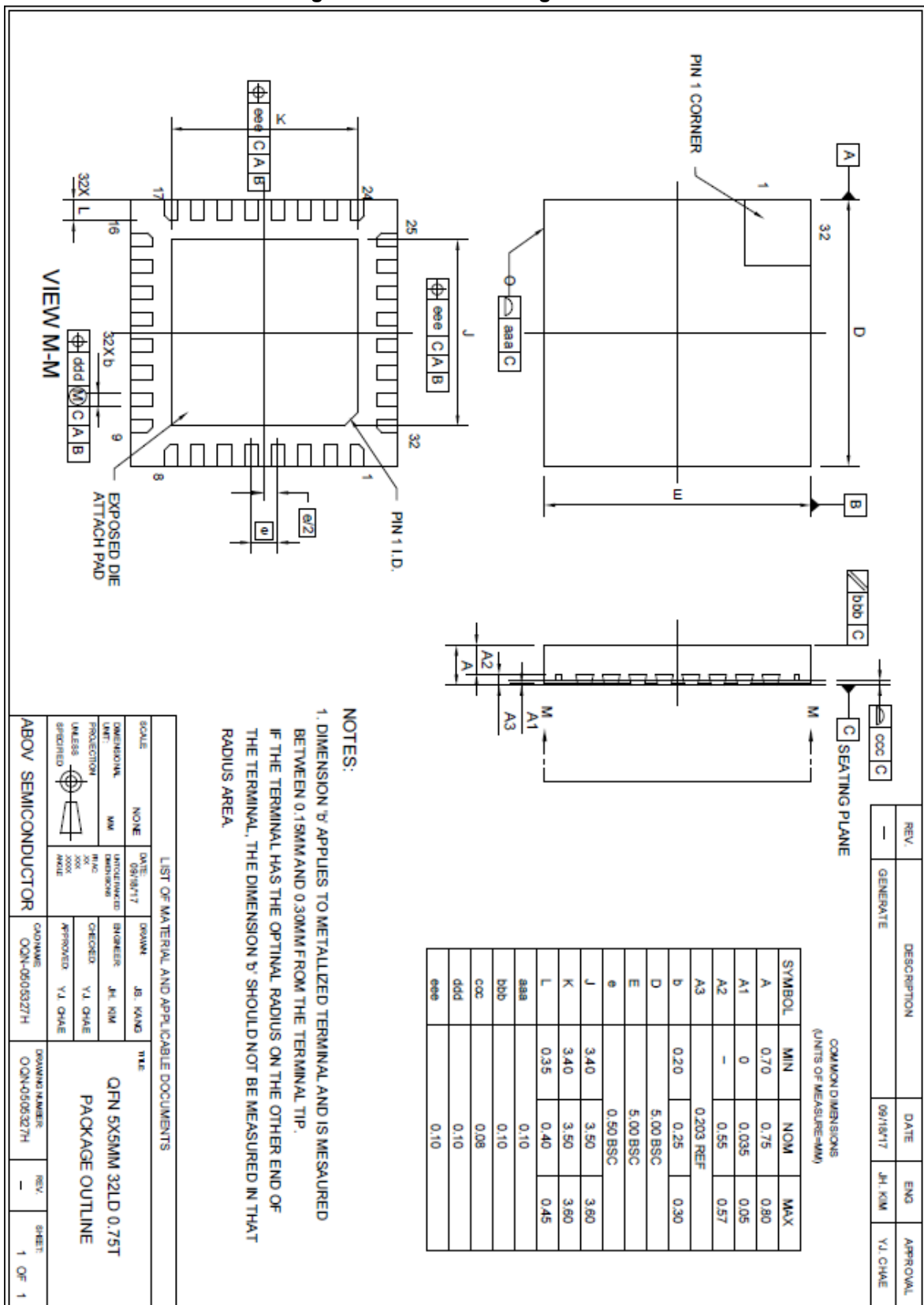
24.1 32-LQFP Package Information

Figure 59. 32-LQFP Package Outline



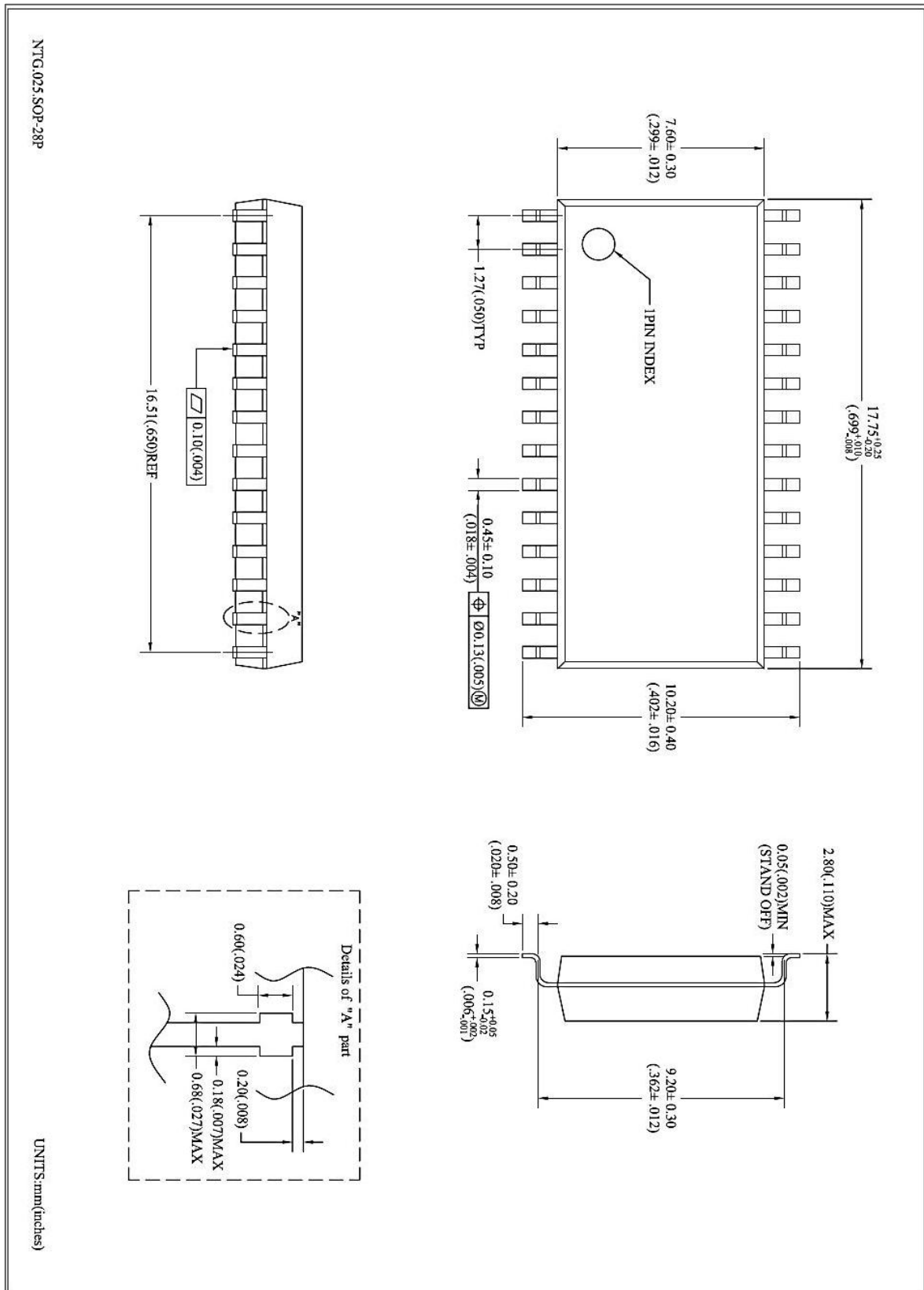
24.2 32-QFN Package Information

Figure 60. 32-QFN Package Outline



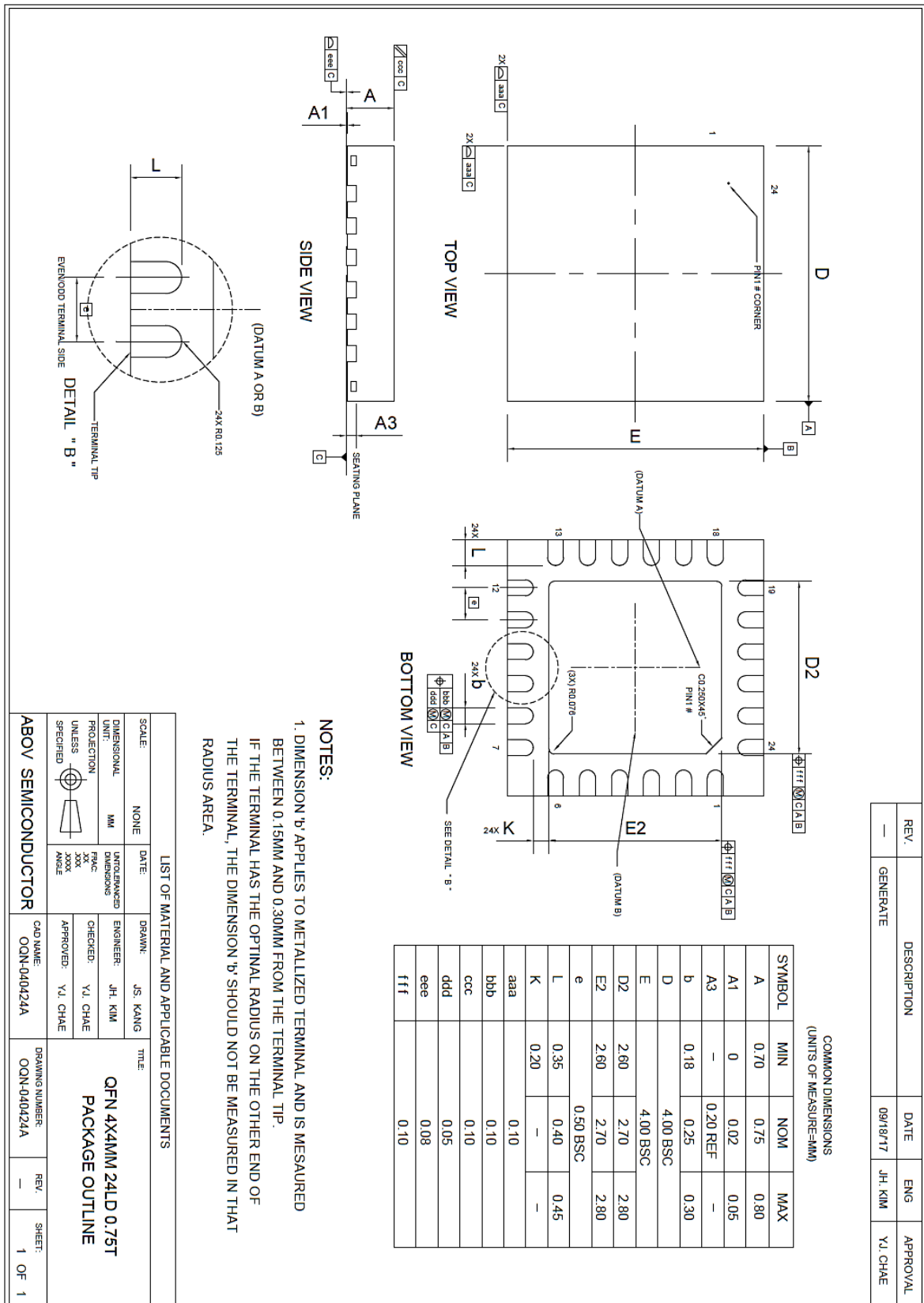
24.3 28-SOP Package Information

Figure 61. 28-SOP Package Outline



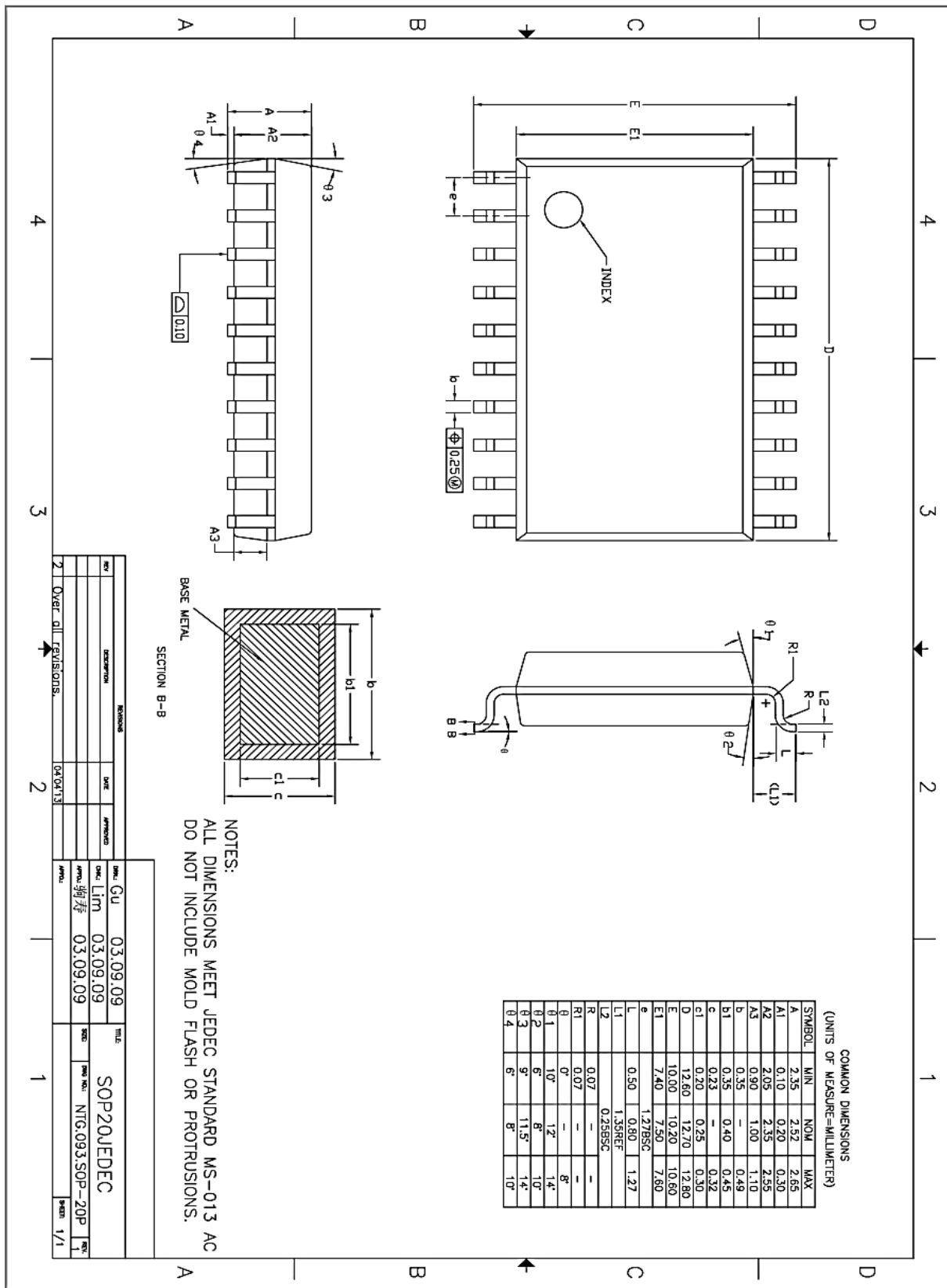
24.4 24-QFN Package Information

Figure 62. 24-QFN Package Outline



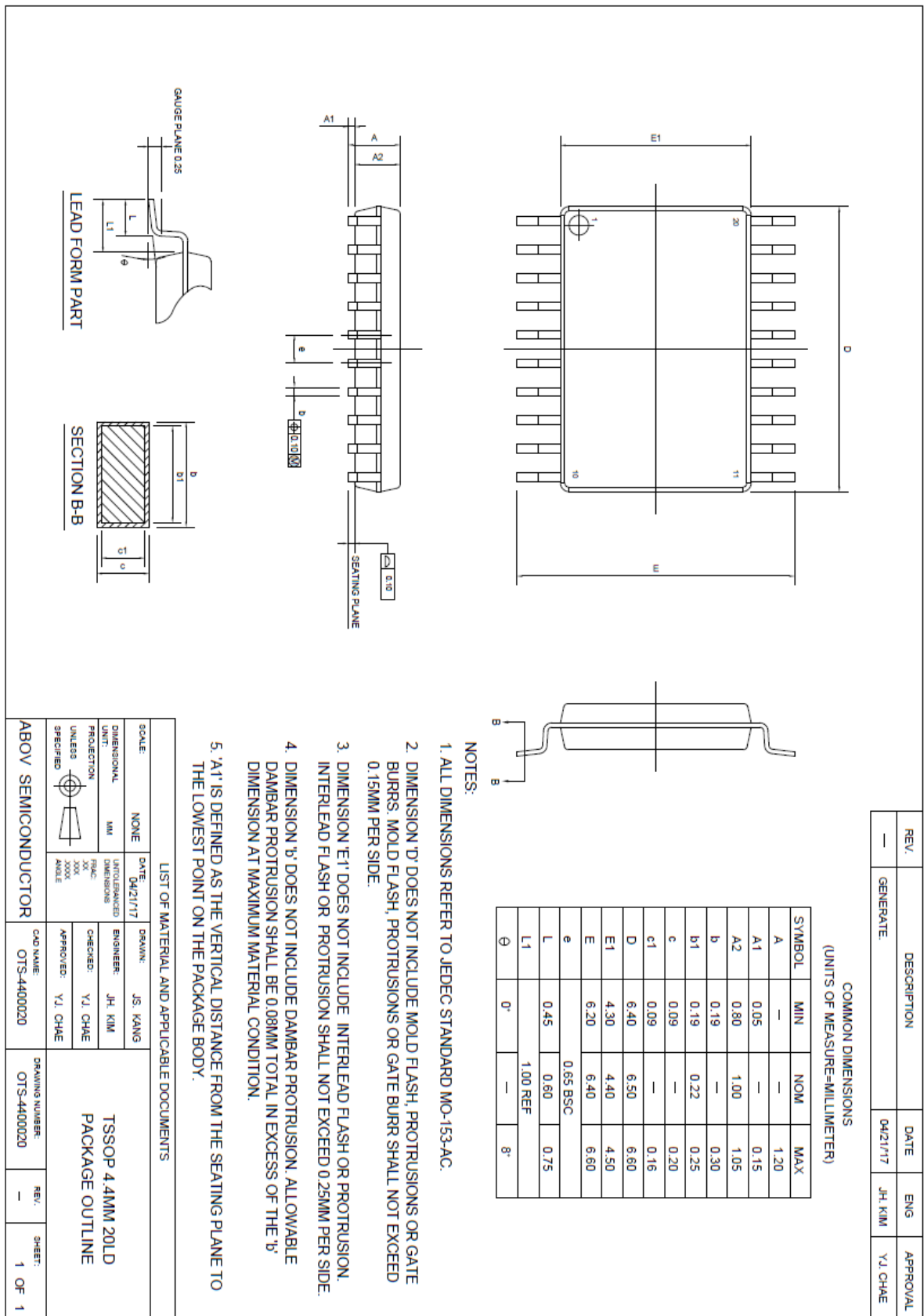
24.5 20-SOP Package Information

Figure 63. 20-SOP Package Outline



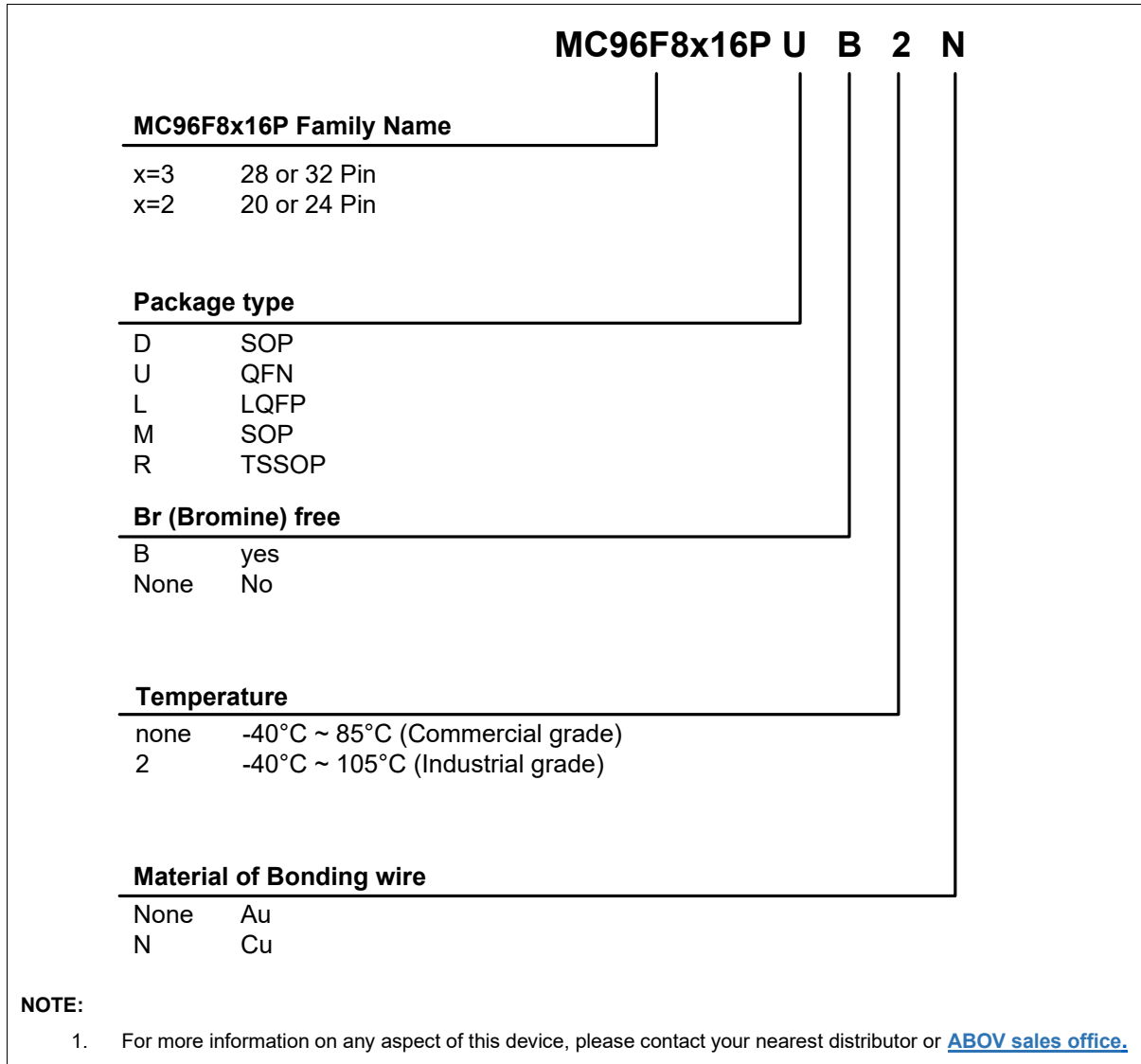
24.6 20-TSSOP Package Information

Figure 64. 20-TSSOP Package Outline



25. Ordering Information

Figure 65. MC96F8x16P Device Numbering Nomenclature



26. Development Tools

This chapter describes a wide range of development tools for MC96F8316P. ABOV offers software tools, debuggers, and programmers to help a user in generating the right results to match target applications. ABOV supports the entire development ecosystem of the customers.

26.1 Compiler

ABOV semiconductor does not provide any compiler for MC96F8316P. However, since MC96F8316P has M8051 as its CPU core, you can use all kinds of third party's standard 8051 compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our OCD emulator and debugger. Please visit our website www.abovsemi.com for more information regarding the OCD emulator and debugger.

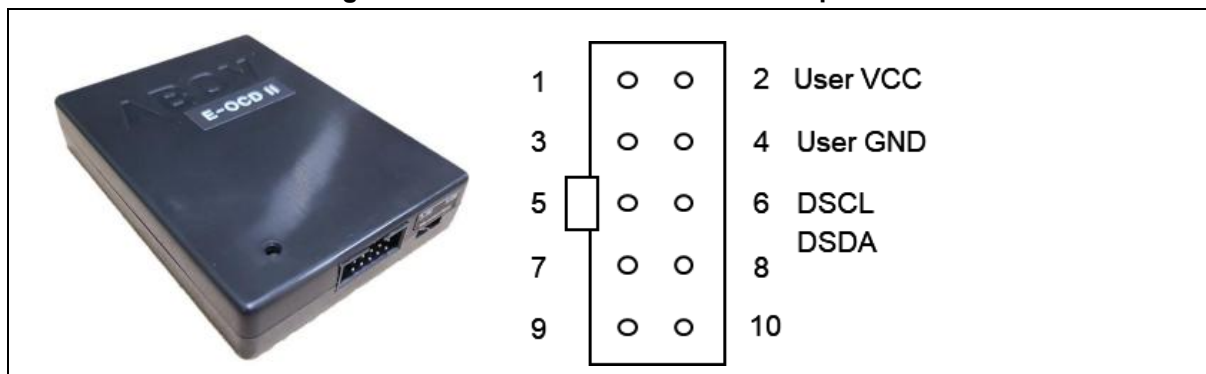
26.2 E-OCD II Interface and OCD Debugger

The E-OCD II interface supports ABOV Semiconductor's 8051 series microcontroller emulation. The E-OCD II uses two wires interfacing between the host computer and microcontroller, which is attached to target system. The E-OCD II can read or change the value of microcontroller's internal memory and I/O peripherals. In addition, the E-OCD II controls microcontroller's internal debugging logic. This means E-OCD II controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10/ 11 (32-bit, 64-bit).

Programming information using the E-OCD II is provided in section 26.5 Circuit Design Guide [Circuit Design Guide](#) later part in this chapter. More detailed information about the E-OCD II, please visit our website www.abovsemi.com and download the debugger software and documents.

Figure 66. E-OCD II and OCD Pin Descriptions



Following is the OCD mode connections:

- DSCl (MC96F8316P P01 port)
- DSDA (MC96F8316P P00 port)

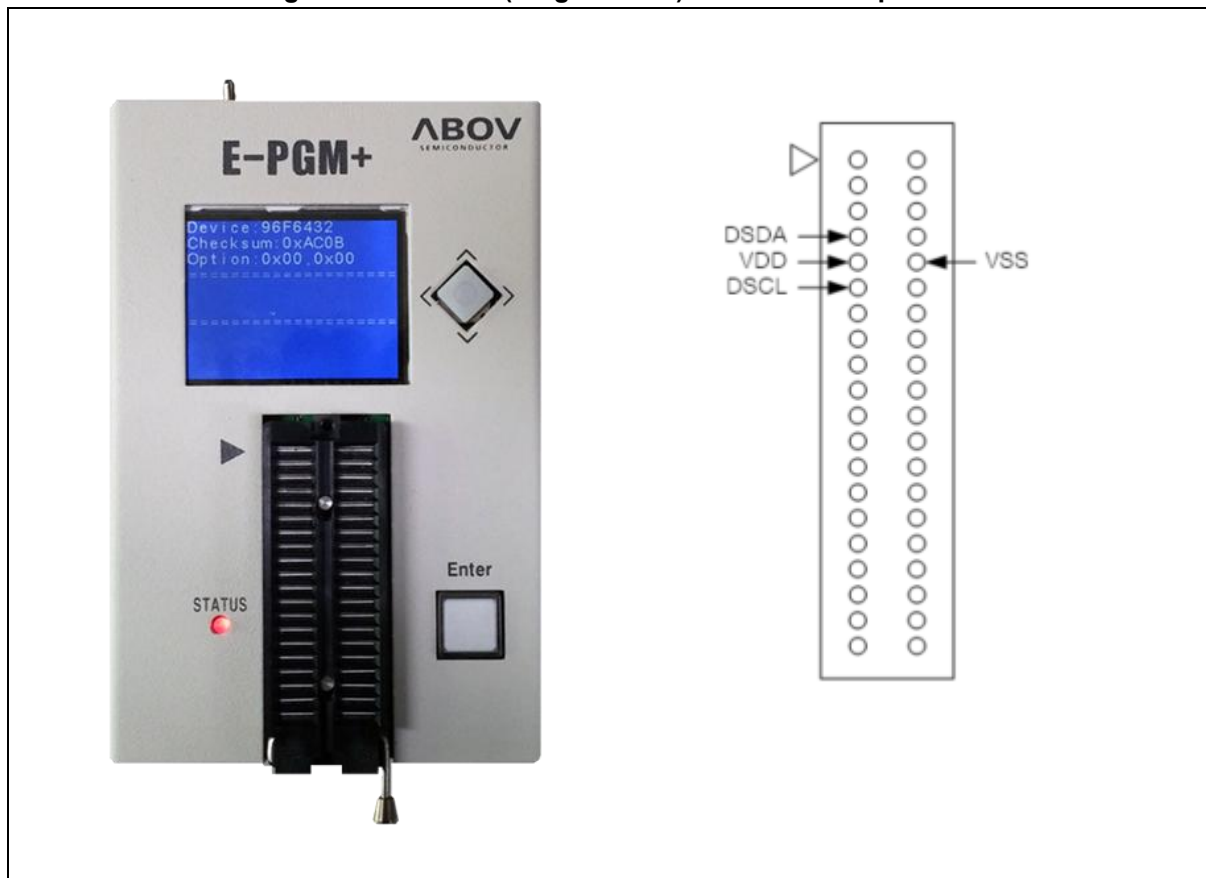
26.3 Programmer

26.3.1 E-PGM+

E-PGM+ is a single programmer and allows a user to program on the device directly.

- Supports for all ABOV microcontroller devices
- Dedicated tool for mass production
- 40-pin Textool DIP socket for single chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls

Figure 67. E-PGM+ (Single Writer) and Pin Descriptions



26.3.2 OCD Emulator

OCD emulator allows a user to write code on the device too, since OCD debugger supports ISP (In-System-Programming). It doesn't require additional hardware, except developer's target system.

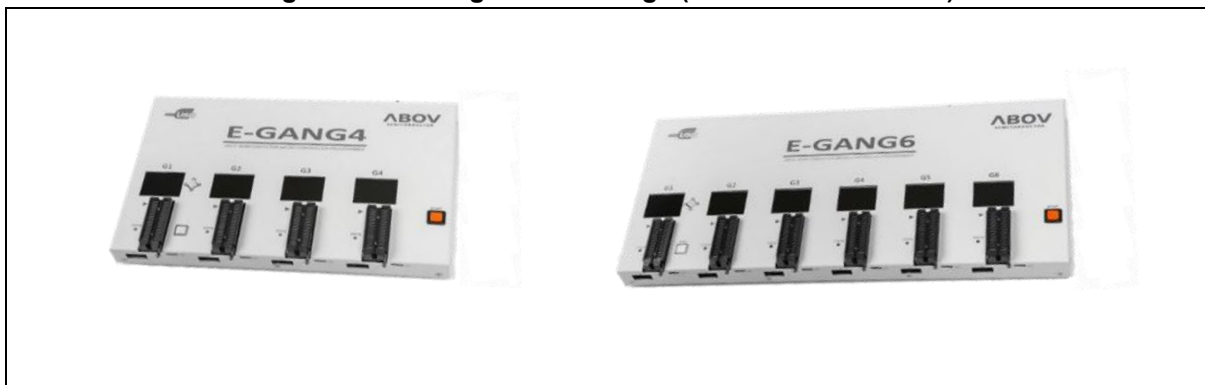
26.3.3 Gang Programmer

E-Gang4 and E-Gang6 allow a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. A USB interface is available, and it is easy to connect to the handler.

Table 36. Specification of E-Gang4 and E-Gang6

Gang Programmer	E-Gang4	E-Gang6
Dimension (x, y, h)	33.5 x 22.5 x 35 mm	148.2 x 22.5 x 35 mm
Weight	2.0 kg	2.8 kg
Input Voltage	DC Adaptor 15 V/2A	DC Adaptor 15 V/2A
Operating Temperature	-10 ~ 40°C	-10 ~ 40°C
Storage Temperature	-30 ~ 80°C	-30 ~ 80°C
Waterproof	No	No

Figure 68. E-Gang4 and E-Gang6 (for Mass Production)



26.4 MTP Programming

Program memory of MC96F8316P is an MTP Type. This Flash is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format. Table 37 describes each pin and corresponding I/O status.

Table 37. Pins for MTP Programming

Pin Name	Main Chip Pin Name	During Programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	–	Logic power supply pin.

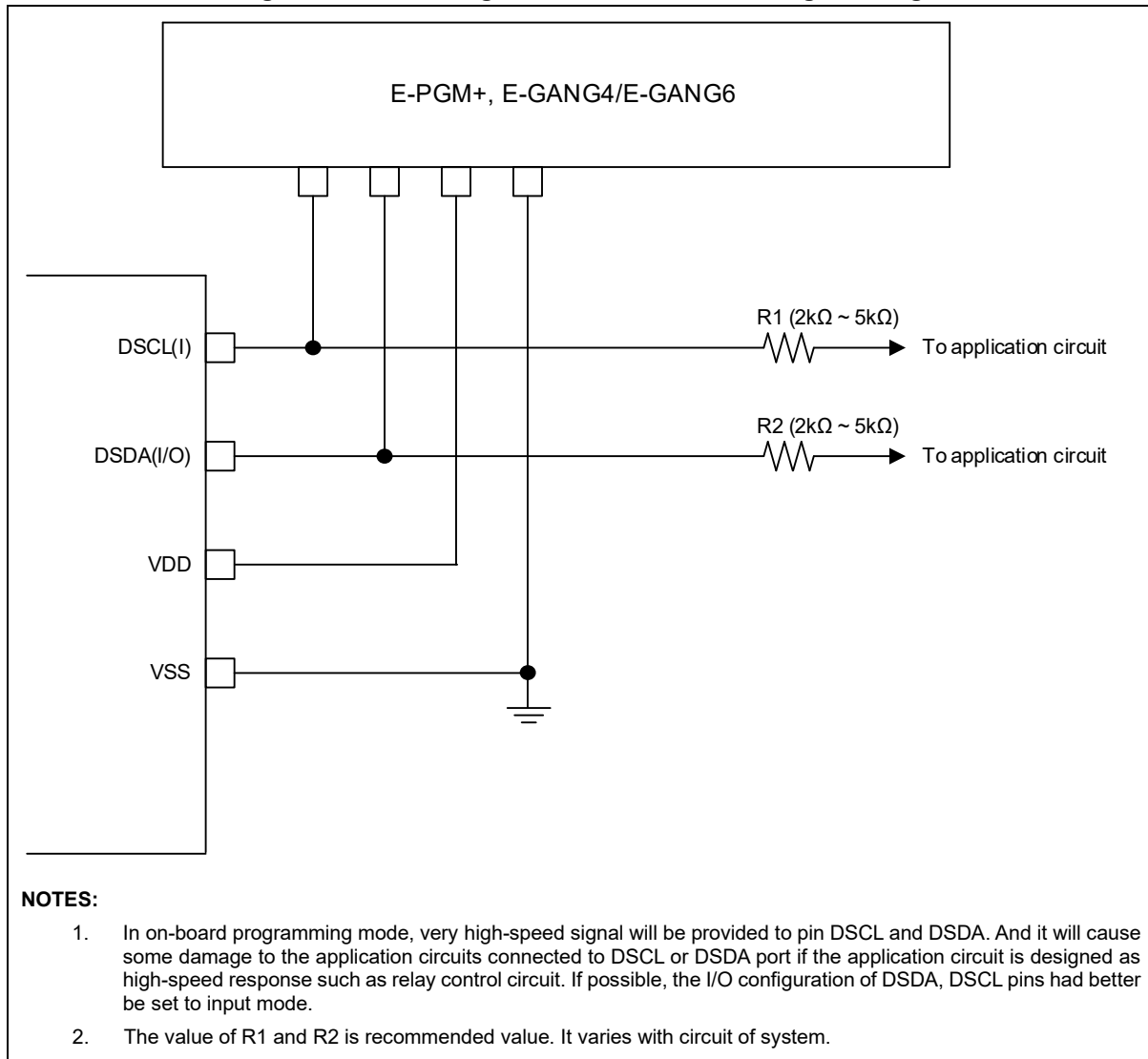
26.4.1 On-board Programming

The MC96F8316P needs only four signal lines including VDD and VSS pins for programming Flash with serial protocol. Therefore, on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

26.5 Circuit Design Guide

When programming Flash memory, the programming tool needs four signal lines, DSCL, DSDA, VDD, and VSS. When you design a PCB circuit, you should consider the usage of these four signal lines for the on-board programming.

Figure 69. PCB Design Guide for On-board Programming



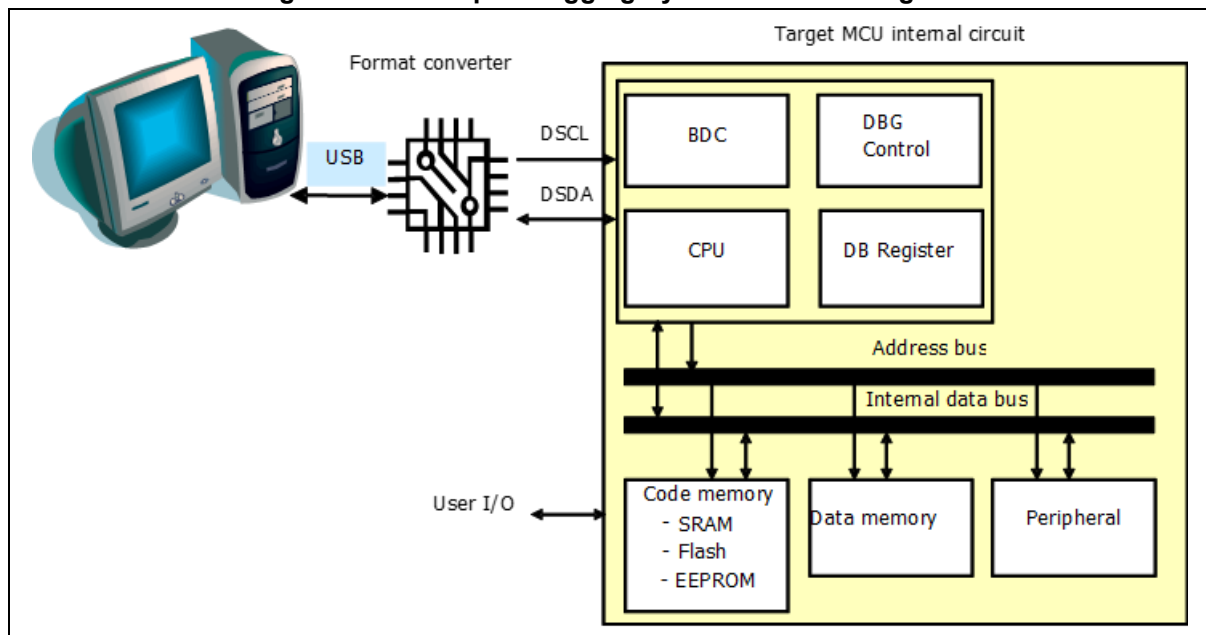
26.5.1 On-chip Debug System

Detail descriptions for programming via the OCD interface can be found in the following figures. Table 38 describes features of OCD and Figure 70 shows a block diagram of the OCD interface and the on-chip Debug system.

Table 38. Features of OCD

Two Wire External Interface	<ul style="list-style-type: none"> • 1 for serial clock input • 1 for bi-directional serial data bus
Debugger Accesses	<ul style="list-style-type: none"> • All internal peripherals • Internal data RAM • Program Counter • Flash memory and EEPROM memory
Extensive On-chip Debugging Supports for Break Conditions	<ul style="list-style-type: none"> • Break instruction • Single step break • Program memory break points on single address • Programming of Flash, Data Flash, Fuses, and Lock bits through the two-wire interface • On-chip Debugging supported by Dr. Choice®
Operating Frequency	The maximum frequency of a target microcontroller.

Figure 70. On-chip Debugging System in Block Diagram

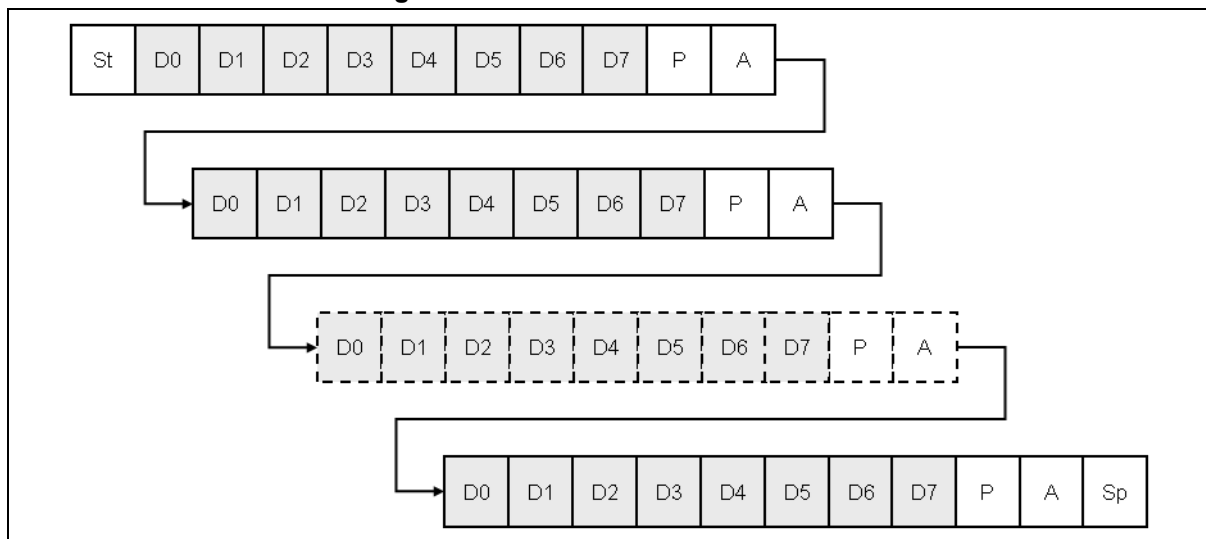


26.5.2 Two-pin External Interface

Basic Transmission Packet

- 10-bit packet transmission using a two-pin interface.
- 1-packet consists of 8-bit data, 1-bit parity and 1-bit acknowledge.
- Parity is even of '1' for 8-bit data in transmitter.
- Receiver generates acknowledge bit as '0' when transmission for 8-bit data and its parity has no error.
- When transmitter has no acknowledge (Acknowledge bit is '1' at tenth clock), error process is executed in transmitter.
- When acknowledge error is generated, host PC makes stop condition and transmits command which has error again.
- The background debugger command is composed of a bundle of packets.
- Start condition and stop condition notify the start and the stop of background debugger command respectively.

Figure 71. 10-bit Transmission Packet



Packet Transmission Timing

Figure 72. Data Transfer on Twin Bus

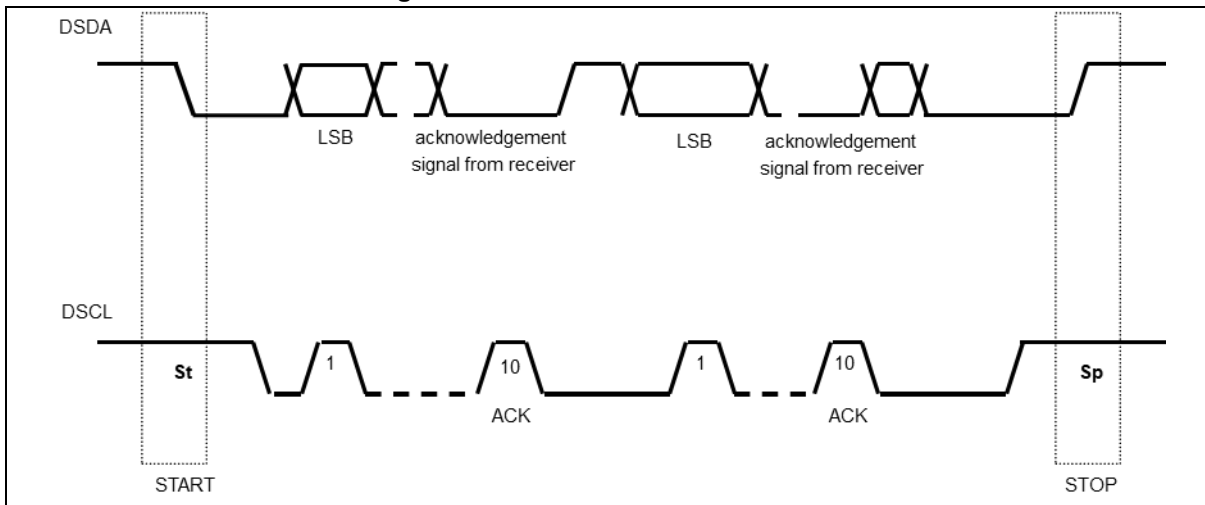


Figure 73. Bit Transfer on Serial Bus

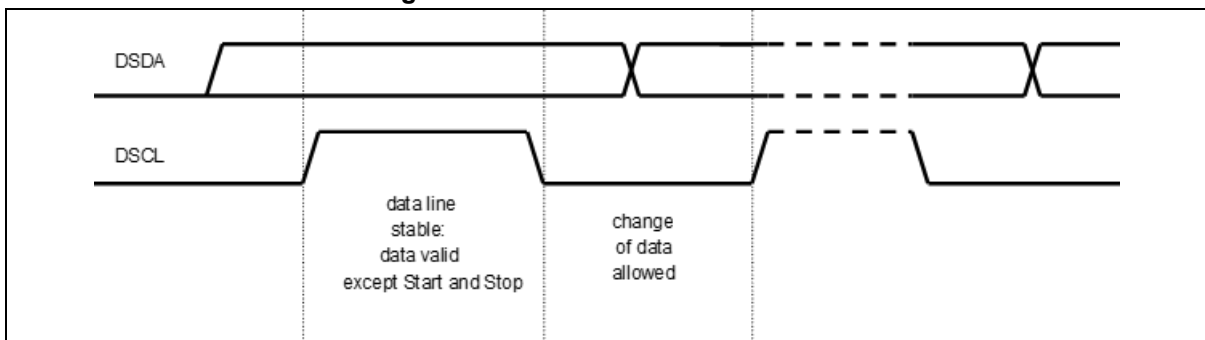


Figure 74. Start and Stop Condition

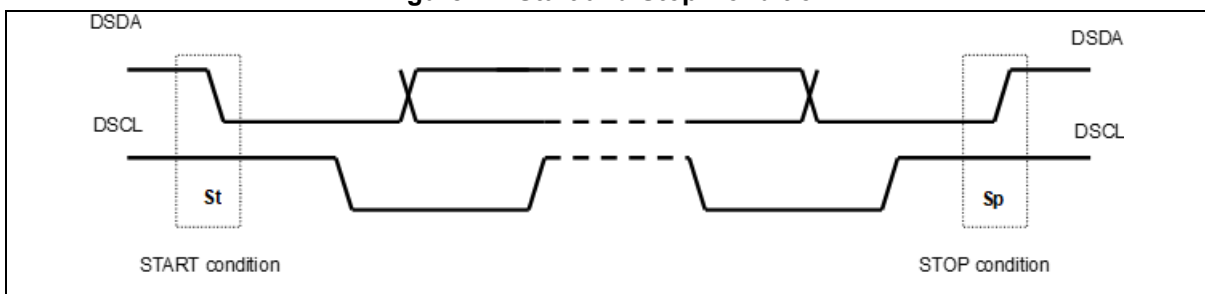


Figure 75. Acknowledge on Serial Bus

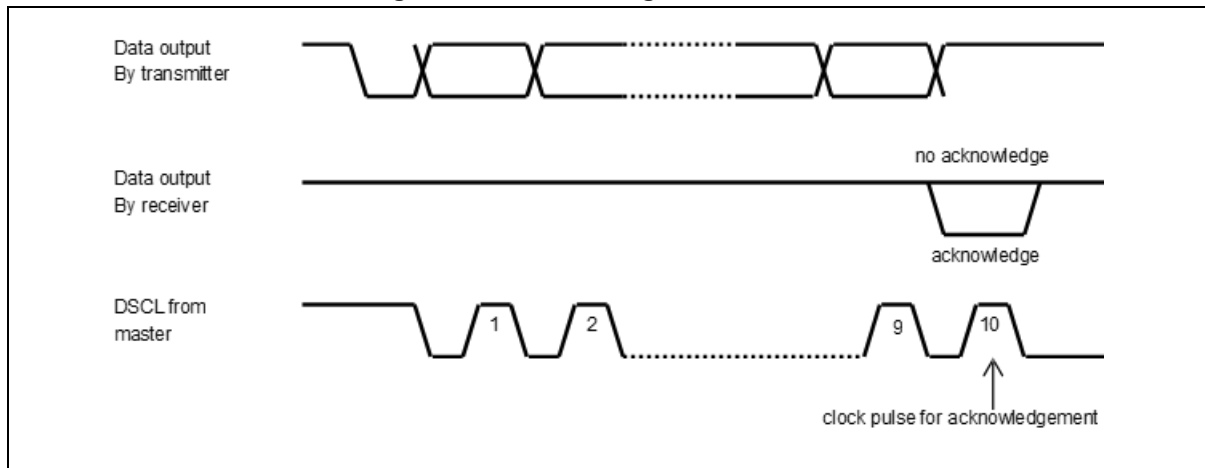
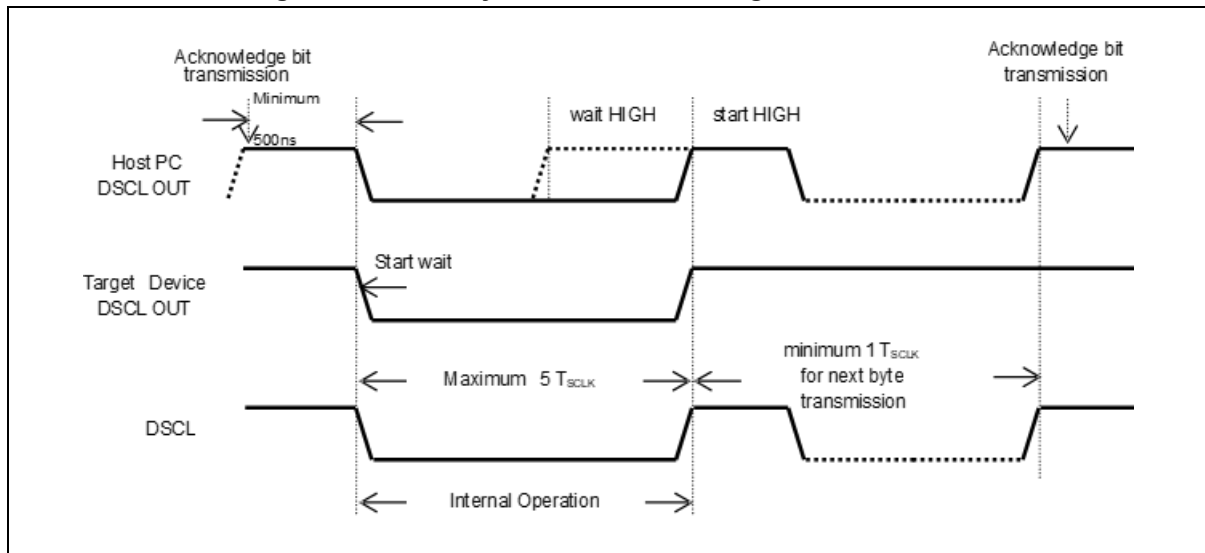


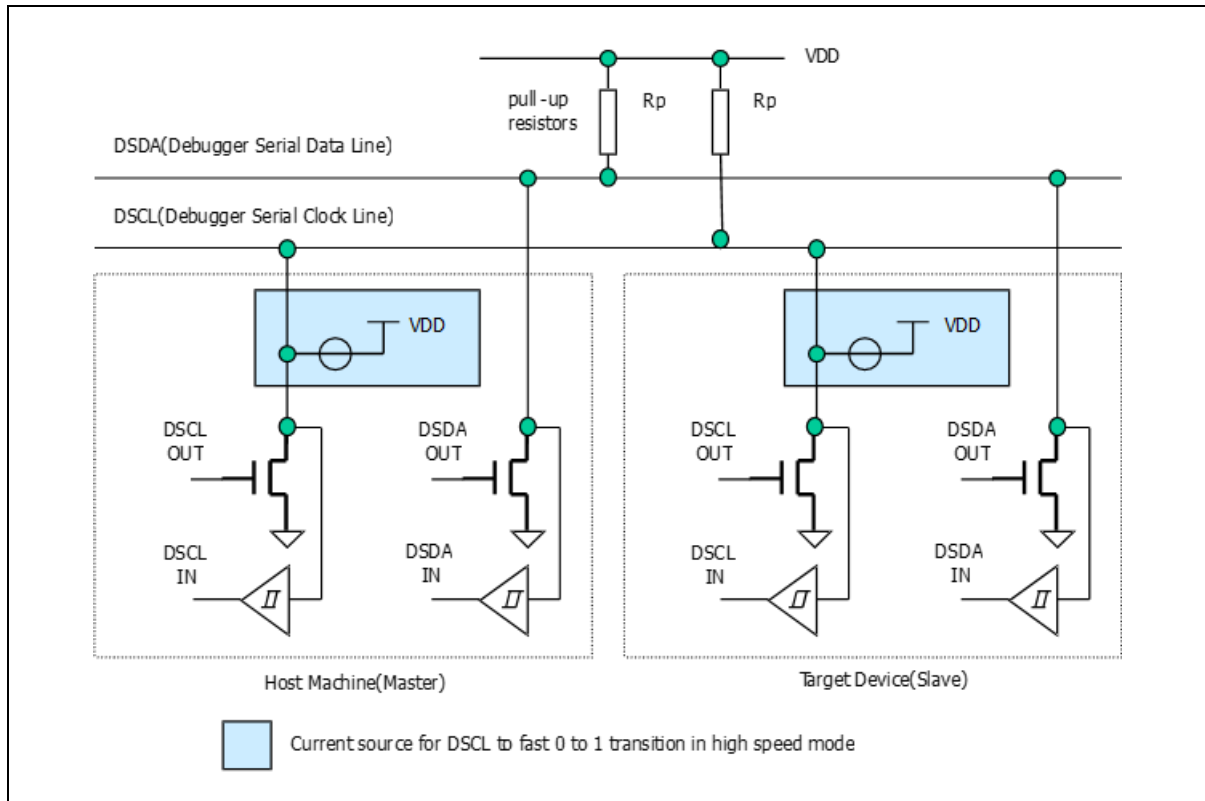
Figure 76. Clock Synchronization During Wait Procedure



26.5.3 Connection of Transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

Figure 77. Connection of Transmission



Appendix

A. Configure Option

Register Description: Configure Option Control

CONFIGURE OPTION 1: ROM Address 001FH

7	6	5	4	3	2	1	0
R_P	HL	–	VAPEN	–	–	–	RSTS

Initial value: 00H

R_P	Code Read Protection
0	Disable
1	Enable
HL	Code Write Protection
0	Disable
1	Enable
VAPEN	Vector Area (00H – FFH) Write Protection
0	Disable Protection (Erasable by instruction)
1	Enable Protection (Not erasable by instruction)
RSTS	Select RESETB pin
0	Disable RESETB pin (P32)
1	Enable RESETB pin

CONFIGURE OPTION 2: ROM Address 001EH

7	6	5	4	3	2	1	0
–	–	–	–	PAEN	PASS2	PASS1	PASS0

Initial value: 00H

PAEN	Enable Specific Area Write Protection		
0	Disable (Erasable by instruction)		
1	Enable (Not erasable by instruction)		
PASS [2:0]	Select Specific Area for Write Protection		
NOTE:			
1. When PAEN = '1', it is applied.			
PASS2	PASS1	PASS0	
0	0	0	0.7 Kbytes (Address 0100H – 03FFH)
0	0	1	1.7 Kbytes (Address 0100H – 07FFH)
0	1	0	2.7 Kbytes (Address 0100H – 0BFFH)
0	1	1	3.7 Kbytes (Address 0100H – 0FFFH)
1	0	0	13.7 Kbytes (Address 0100H – 37FFH)
1	0	1	14.7 Kbytes (Address 0100H – 3BFFH)
1	1	0	15.2 Kbytes (Address 0100H – 3DFFH)
1	1	1	15.5 Kbytes (Address 0100H – 3EFFH)

B. Instruction Table

- Instructions are either 1, 2 or 3 bytes long as listed in the 'Bytes' column in tables shown below.
- Each instruction takes either 1, 2 or 4 machine cycles to execute as listed in the following tables in this section.
- 1 machine cycle comprises 2 system clock cycles.

Table 39. Instruction Table: Arithmetic

Arithmetic				
Mnemonic	Description	Bytes	Cycles	Hex Code
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	05
INC @Ri	Increment indirect memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	1	16-17
INC DPTR	Increment data pointer	1	2	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	4	84
DAA	Decimal Adjust A	1	1	D4

Table 40. Instruction Table: Logical

Logical				
Mnemonic	Description	Bytes	Cycles	Hex Code
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13

Table 41. Instruction Table: Data Transfer

Data Transfer				
Mnemonic	Description	Bytes	Cycles	Hex Code
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7

Table 42. Instruction Table: Boolean

Boolean				
Mnemonic	Description	Bytes	Cycles	Hex Code
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0
MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92

Table 43. Instruction Table: Branching

Branching				
Mnemonic	Description	Bytes	Cycles	Hex Code
ACALL addr 11	Absolute jump to subroutine	2	2	11→F1
LCALL addr 16	Long jump to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5

Table 44. Instruction Table: Miscellaneous

Miscellaneous				
Mnemonic	Description	Bytes	Cycles	Hex Code
NOP	No operation	1	1	00

Table 45. Instruction Table: Additional Instructions

Additional instructions (selected through EO[7:4])				
Mnemonic	Description	Bytes	Cycles	Hex Code
MOVC @ (DPTR++),A	M8051W/M8051EW-specific instruction supporting software download into program memory	1	2	A5
TRAP	Software break command	1	1	A5

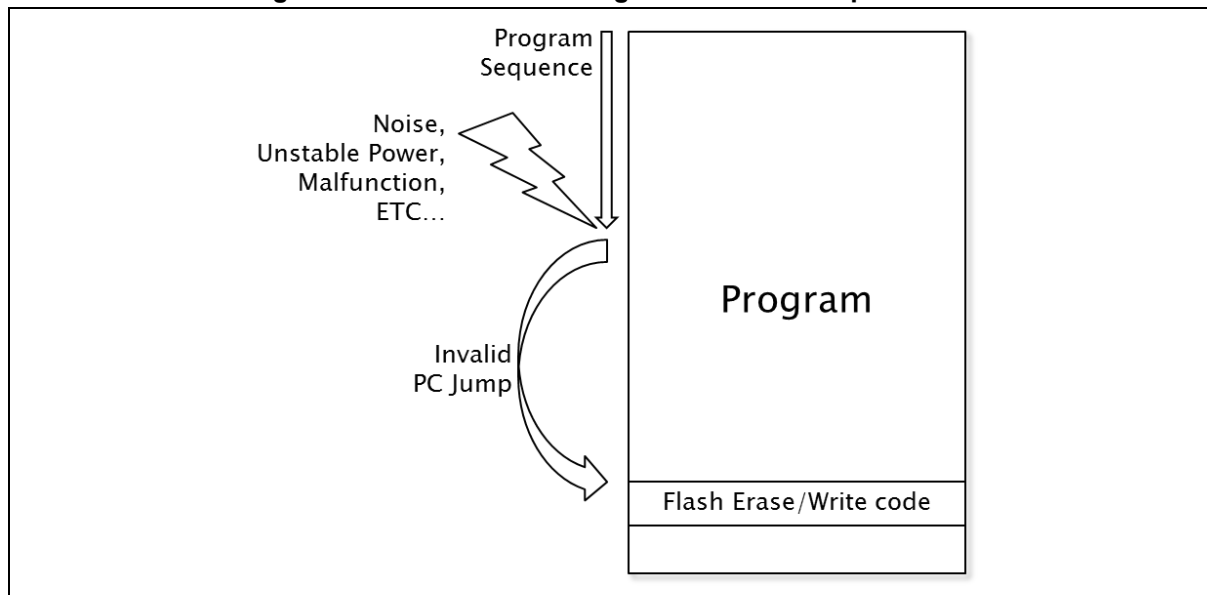
In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, and the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11→F1 (for example), are used for absolute jumps and calls, with the top 3 bits of the code being used to store the top three bits of the destination address.

The CJNE instructions use the abbreviation #d for immediate data; other instructions use #data.

C. Flash Protection for Invalid Erase/Write

Appendix C shows example code to prevent code or data from being changed by abnormal operations such as noise, unstable power, and malfunction.

Figure 78. Flash Protection against Abnormal Operations



How to Protect Flash

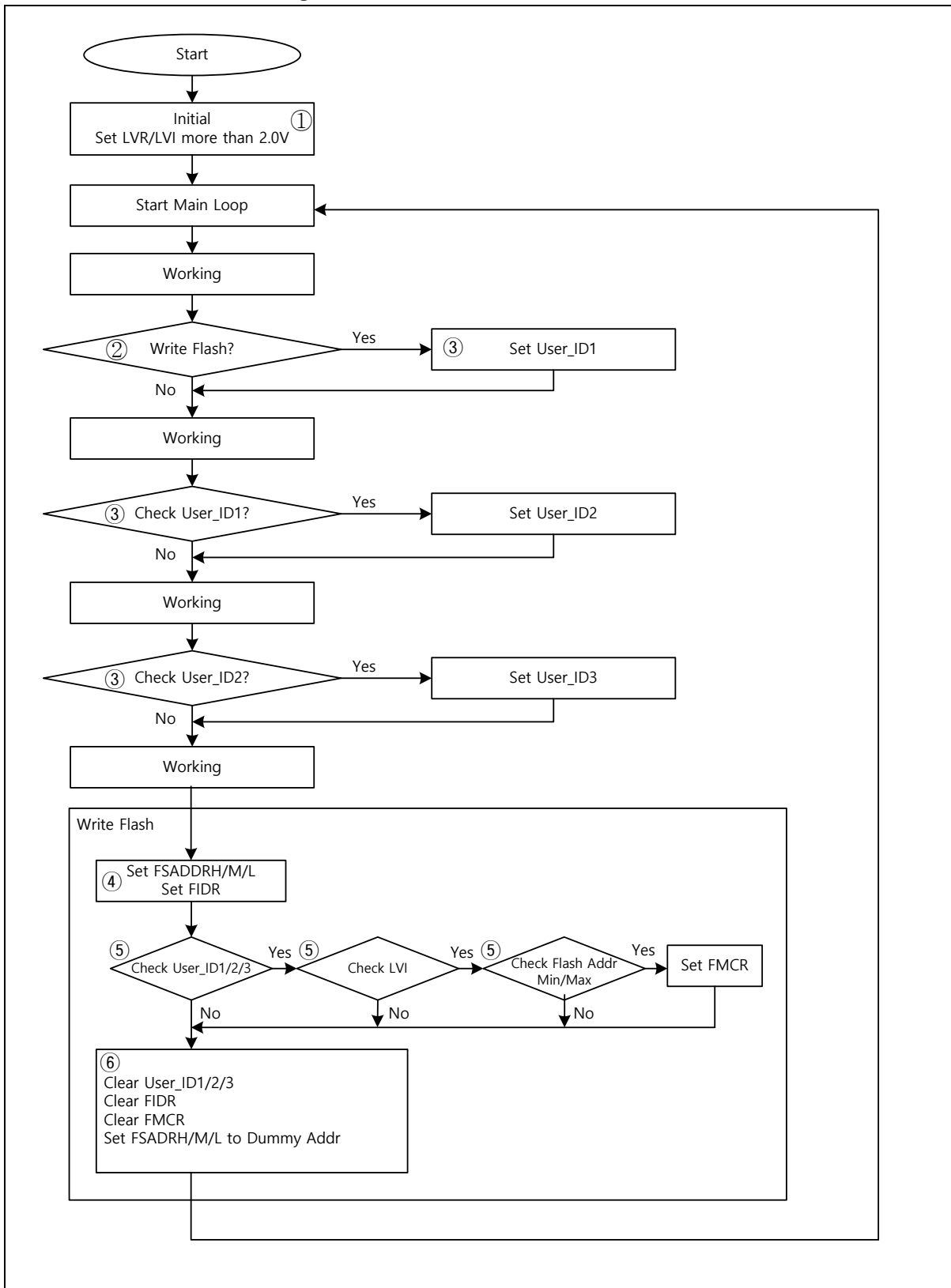
- Divide into decision and execution to Erase/Write in Flash.
 - Check the program sequence from decision to execution in order of precedence about Erase/Write.
 - Setting the flags in program and check the flags in main loop at the end
 - When the Flash Erase/Write is executed, check the flags. If not matched, do not execute.
- Check the range of Flash Sector Address
 - If the Flash sector address is outside of specific area, do not execute.
- Use the Dummy Address
 - Set the Flash sector address to dummy address in usually run time.
 - Change the Flash sector address to real area range shortly before Erase/Write.
 - Even if invalid Erase/Write occurred, it will be Erase/Write in dummy address in Flash.
- Use the LVR/LVI
 - Unstable or low powers give an adverse effect on microcontrollers. So, use the LVR/LVI.

Protection Flow Description

The Flash protection procedure is described in flowchart in Figure 79, and each step in this figure is described in the following lists:

1. Initialization
 - Set the LVR/LVI. Check the power by LVR/LVI and do not execute under unstable or low power.
 - Initialize User_ID1/2/3
 - Set Flash Sector Address High/Middle/Low to Dummy address. Dummy address is set to unused area range in Flash.
2. Decide to Write
 - When the Erase/Write are determined, set flag. Do not directly Erase/Write in Flash.
 - Make the user data.
3. Check and Set User_ID1/2/3
 - In the middle of source, insert code which can check and set the flags.
 - By setting the User_ID 1/2/3 sequentially and identifying the flow of the program.
4. Set Flash Sector Address
 - Set address to real area range shortly before Erase/Write in Flash.
 - Set to Dummy address after Erase/Write. Even if invalid work occurred, it will be Erase/Write in Dummy address in Flash.
5. Check Flags
 - If every flag (User_ID1/2/3, LVI, Flash Address Min/Max) was set, then do Erase/Write.
 - If the Flash Sector Address is outside of Min/Max, do not execute
 - Address Min/Max is set to unused area.
6. Initialize Flags
 - Initialize User_ID1/2/3
 - Set Flash Sector Address to Dummy Address
- Sample Source
 - Refer to the ABOV website (www.abovsemi.com).
 - Each product should be modified according to the Page Buffer Size and Flash Size

Figure 79. Flowchart of Flash Protection



Other Protection by Configure Options

- Protection by Configure option
 - Set Flash protection by microcontroller Write Tool (OCD, PGM+, etc.)
 - Vector Area: 00H~FFH
 - Specific Area (MC96F8316P):
 - 0.7 KBytes (Address 0100H – 03FFH)
 - 1.7 KBytes (Address 0100H – 07FFH)
 - 2.7 KBytes (Address 0100H – 0BFFH)
 - 3.8 KBytes (Address 0100H – 0FFFH)
 - 13.7 KBytes (Address 0100H – 37FFH)
 - 14.7 KBytes (Address 0100H – 3BFFH)
 - 15.2 KBytes (Address 0100H – 3DFFH)
 - 15.5 KBytes (Address 0100H – 3EFFH)
 - The range of protection may be different for each product.

Revision History

Revision	Date	Description
1.00	Jul. 23, 2024	Initial release
1.01	Dec. 2, 2024	Updated the disclaimer.
1.10	Jul. 14, 2025	<ul style="list-style-type: none">• Added 20-TSSOP package.• Corrected typos.

Korea**Regional Office, Seoul
R&D, Marketing & Sales**

8th Fl., 330, Yeongdong-daero, Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200

Fax: +82-2-508-6903

www.abovsemi.com

**HQ, Ochang
R&D, QA, and Test Center**

37, Gangni 1-gil, Ochang-eup, Cheongwon-gun,
Chungcheongbuk-do, 28126, Korea

Tel: +82-43-219-5200

Fax: +82-43-217-3534

www.abovsemi.com

Domestic Sales Manager

Tel: +82-2-2193-2206

Fax: +82-2-508-6903

Email: sales_kr@abov.co.kr

Global Sales Manager

Tel: +82-2-2193-2281

Fax: +82-2-508-6903

Email: sales_gl@abov.co.kr

China Sales Manager

Tel: +86-755-8287-2205

Fax: +86-755-8287-2204

Email: sales_cn@abov.co.kr

Japan Sales Manager

Tel: +81-50-6883-8679

Email: sales_jp@abov.co.kr

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