A31S134 Datasheet

Cortex®-M0+ 32MHz General-Purpose Microcontroller with 128K + 4KB FlashRom and 16KB SRAM

DS Rev. 1.04

Features

Core

- Arm® Cortex®-M0+ 32-bit core
- Up to 32 MHz clock speed

Memory

- 128 KB code flash memory
  - Read protection for security
- 4 KB data flash memory
  - Read protection for security
- 16 KB SRAM

Clock, Reset and Power Management

- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Low-Voltage Detection
  - Low-Voltage Reset (LVR)
  - Low-Voltage Indicator (LVI)
- Power management for power consumption
  - Run, SLEEP, DEEP-SLEEP modes
- Clock monitoring function for system clock

Interrupt Management

- Nested-Vectored Interrupt Controller (NVIC) with 28 interrupt sources

General-Purpose Input/Output

- Up to 61 I/O pins
- 32 mappable on external interrupt vectors
- Sink type high-current output ports

DMA Controller

- Two channels of Direct Memory Access
- 8-/ 16-/ 32-bit data transfers
- Conjunction with 20 internal peripherals

ADC

- One independent ADC block
- 14 analog input channels
- 5-bit prescaler
- 50 ksps conversion rate

Timer

- 16-bit timers: 6 channels
- 32-bit timers: 2 channels
- Timer operating modes
  - Periodic timer mode
  - One-shot mode
  - PWM mode
  - Capture mode
- 12-bit prescaler

WatchDog Timer

- 24-bit down-count timer
- Reset and periodic interrupts
- Four dividers selectable

Watch Timer

- 14-bit divider
- 12-bit up counter
- Real-Time Clock

Communication Interfaces

- UART
  - Two Universal Asynchronous serial Receiver-Transceiver ports
- USART
  - Three Universal Synchronous Asynchronous Serial Receiver-Transceiver ports
- I2C
  - Three Inter-Integrated Circuit interface ports
- SPI
  - Two Serial Peripheral Interface ports

CRC Calculation Unit

- CRC operating modes:
  - CRC-CCITT
  - CRC-16
  - Auto CRC / User-defined CRC
  - CRC and checksum

Debug Interface

- Serial Wire Debug (SWD) interface

Package

- 64-LQFP-1010 (0.50 mm pitch)
- 48-LQFP-0707 (0.50 mm pitch)
- 44-LQFP-1010 (0.80 mm pitch)
- 32-LQFP-0707 (0.80 mm pitch)
- 32-QFN-0505 (0.50 mm pitch)

Operating Voltage

- 1.8 V to 5.5 V

Operating Temperature

- Commercial grade (−40°C to 85°C)
- Industrial grade (−40°C to 105°C)

Product Selection Table

Table 1. Device Series Summary

Base Product	Part Number	Flash	SRAM	UART	USART	SPI	I2C	ADC	Timer	I/O ports	Package
A31S134	A31S134RL	128 KB	16 KB	2	3	2	3	14	8	61	64-LQFP-1010
	A31S134CL	128 KB	16 KB	2	3	2	3	14	8	45	48-LQFP-0707
	A31S134SN	128 KB	16 KB	2	3	2	3	14	8	41	44-LQFP-1010
	A31S134KN	128 KB	16 KB	1	3	2	2	8	8	29	32-LQFP-0707
	A31S134KU	128 KB	16 KB	1	3	2	2	8	8	29	32-QFN-0505

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1. Introduction

This document provides an overview of the features supported by the device, including high-level information and brief explanations for each feature. Refer to Table 3 for the list of features supported by the device.

2. Description

The A31S134 is a 32-bit microcontroller based on the energy efficient Arm Cortex-M0+ core, with up to 128 KB of code flash memory, 4 KB of data flash memory, and 16 KB of SRAM. The A31S134 operates at voltage range of 1.8 V to 5.5 V, providing a highly flexible and cost-effective solution for many embedded control applications. It features a variety of peripherals, including 16-bit and 32-bit timers, a 12-bit ADC, a CRC generator, as well as UART, USART, I2C, SPI, and DMA. In addition, the device is equipped with a POR, LVR, LVI, and an internal RC oscillator. To further reduce power consumption, the A31S134 supports both SLEEP and DEEP-SLEEP modes.

2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for the A31S134.

Table 2. A31S134 Memory Capacity

Memory Capacity		Category
Flash	RAM	
128 KB	16 KB	A31S134

2.2 Device Overview

Table 3 summarizes and lists the features specific to the device while considering the largest package.

Table 3. A31S134 Features and Peripherals

Item		Description
Core	CPU	• Max. operating frequency: 32 MHz • 32-bit Arm Cortex-M0+ core • 16-bit Thumb-2 instruction set • Register settings in CPU: - General-purpose registers: R0 - R12 - Main Stack Pointer (MSP) and Process Stack Pointer (PSP): R13 - Link Register (LR): R14 - Program Counter (PC): R15 • Data alignment in little-endian • AHB / APB
	Interrupt Controller	• Nested-Vectored Interrupt Controller (NVIC) • Max. 28 peripheral interrupts available • Two-bit width of group priority: four levels of priority
Memory	Code Flash	• Capacity: 128 KB • Large volume of embedded code flash memory • Max. 32 MHz flash access speed • Erase unit: Page (256-byte), Bulk (128 KB, full-chip) • Program unit: Word (4-byte), Page (256-byte) • Read protection • Self-programming • CRC code generation and verification for the flash memory • Endurance: 10,000 cycles • Lifetime: 10 years
	Data Flash	• Capacity: 4 KB • Max. 32 MHz access speed • Erase unit: Page (32-byte), Bulk (4 KB) • Program unit: Word (4-byte), Page (32-byte) • Read protection • Endurance: 100,000 cycles • Lifetime: 10 years
	SRAM	• Capacity: 16 KB • Capable of functioning as a program's working area • High-speed execution for time-critical codes • Capability to remap into an interrupt vector area

Table 3. A31S134 Features and Peripherals (continued)

Item		Description
System Control Unit (SCU)	Operating Frequency	• 2 MHz to 32 MHz (HIRC, XMOSC)
	Clock	• High-frequency Internal Resistor-Capacitor (IRC) oscillator - 32 MHz (±1.5% @ Ta = 0°C to 50°C) • External Main Oscillator (XMOSC) - 16 MHz @ VDD = 2.7 V to 5.5 V • External Sub-Oscillator (XSOSC) - 32.768 kHz @ VDD = 1.8 V to 5.5 V
	Clock Monitoring	• System fail-safe function by clock monitoring - External main oscillator - External sub-oscillator - Main system clock (MCLK)
	Operation Mode	• RUN mode • SLEEP mode • DEEP-SLEEP (STOP) mode
	Reset	• nRESET pin reset • Power-On Reset (POR) • Software reset • Watch Dog Timer Reset (WDTR) • Low-Voltage Reset (LVR) • Clock monitoring reset
	VDC	• Low-dropout (LDO) regulator built in for low-voltage operation
	POR	• POR generator: Capable of generating a reset signal by detecting an internal 1.2 V
	LVI	• 12 low-voltage detection levels • Supports interrupt • Supports wake-up from SLEEP mode
	Wake-up	• Wake-up by General-Purpose Input / Output (GPIO) interrupt pin • Wake-up by Watch Timer (WT) • Wake-up by Watchdog Timer (WDT) • Wake-up by Timer 20 (T20) • Wake-up by Low-Voltage Indicator (LVI)
	Wake-Up Timer (WUT)	• 16-bit down-count timer • Underflow interrupt • Stabilization time upon wake-up from deep sleep mode

Table 3. A31S134 Features and Peripherals (continued)

Item	Description
General-Purpose I/O (GPIO)	• Input/Output (I/O) port for general purpose • 64-LQFP-1010 - I/O pins: 61 • 48-LQFP-0707 - I/O pins: 45 • 44-LQFP-1010 - I/O pins: 41 • 32-LQFP-0707 - I/O pins: 29 • 32-QFN-0505 - I/O pins: 29 • Selectable input and output configuration for each pin: - Push-pull output - Open drain output - Input • Pin configurations through multiplexer settings • Configurable as an external interrupt source (PB[11:0], PC[7:0], PE[8:0], PF[4:2]) with the following options: - Rising edge (high-level) - Falling edge (low-level) - Edge-triggered (both rising- and falling-edge) • Configurable pull-up/down resistors and debouncing • Configurable independently to be set or reset through its corresponding bit • Wake-up events triggered by external asynchronous interrupt inputs
LED Display Driver	• Sink up to 120 mA of current for driving up to 8 pins - PD0 to PD7
Direct Memory Access (DMA) Controller	• Two-channel Direct Memory Access (DMA) supporting peripherals • 8- / 16- / 32-bit data transfers • Compatible with 20 different types of peripherals - USART10, USART11, USART12 - UART0, UART1 - I2C0, I2C1, I2C2 - SPI0, SPI1

Table 3. A31S134 Features and Peripherals (continued)

Item		Description
General-Purpose Timer	16-bit Timer	• General-purpose 16-bit up-count timer • Six channels - Six capture input pins (T1nCAP) - Six output pins (T1nOUT) • Timer operating modes - Periodic timer mode - Capture mode - PPG one-shot mode - PPG repeat mode • Interrupt events - Timer / counter match interrupt - Capture interrupt • Freely selectable clock sources: - PCLK clock divided by 12-bit prescaler - External clock
	32-bit Timer	• General-purpose 32-bit up-count timer • Two channels - Two input capture (T2nCAP) channels - Two output (T2nOUT) channels • Timer operating modes - Periodic timer mode - Capture mode - PPG one-shot mode - PPG repeat mode • Interrupt events - Timer/counter match interrupt - Capture interrupt • Freely selectable clock sources: - PCLK clock divided by 12-bit prescaler - External clock (T20, T21) - XSOSC clock (T20) • Timer signals output through T2nOUT output pins
System Timer	WatchDog Timer	• 24-bit down-count timer • Reset generation • Window match interrupt • Underflow interrupt • WDTRC or PCLK is selectable
	Watch Timer	• 12-bit up-count timer • Real-Time Clock (RTC)

Table 3. A31S134 Features and Peripherals (continued)

Item		Description
Communication Interface	UART	• Two asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming - 5- to 8-bit data transfers - Even / Odd / Non-parity generation and checking - 1-bit, 1.5-bit, or 2-bit stop bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	USART	• Three asynchronous / synchronous serial communication ports • Flexible communication available through programming - Full duplex operation with independent serial receive and transmit registers - Supports serial frames with 5 to 9-bit data transfer lengths and 1 or 2 stop bits generation and checking - Even / Odd / Non-parity generation and checking - Baud rate generator - Receive character detection and receive time-out function • UART, LIN, and SPI modes
	SPI	• Two synchronous serial communication ports • Master / slave operation • Loop-back mode • Programmable and flexible communication - SPI clock speed • Both Least Significant Bit (LSB)-first and Most Significant Bit (MSB)-first modes available
	I2C	• Three serial communication ports • Standard I2C communication protocol • Master and slave modes • 7-bit addressing for slave mode • Configurable SCL signal's high / low periods • Configuable SDA signal's hold time
12-bit A/D Converter (ADC)		• 14 analog input channels • Software and timer triggers • External reference selectable
Cyclic Redundancy Check (CRC)		• 16-bit CRC generator • CRC operating modes: - CRC-CCITT - CRC-16 • Auto and user mode supported • CRC and Checksum generation

Table 3. A31S134 Features and Peripherals (continued)

Item		Description
Operating Voltage		• 1.8 V to 5.5 V
Operating Temperature	Commercial Grade	• −40°C to 85°C
	Industrial Grade	• −40°C to 105°C
Package		• Five types of package options - 64-LQFP-1010 (0.5 mm pitch) - 48-LQFP-0707 (0.5 mm pitch) - 44-LQFP-1010 (0.8 mm pitch) - 32-LQFP-0707 (0.8 mm pitch) - 32-QFN-0505 (0.5 mm pitch)

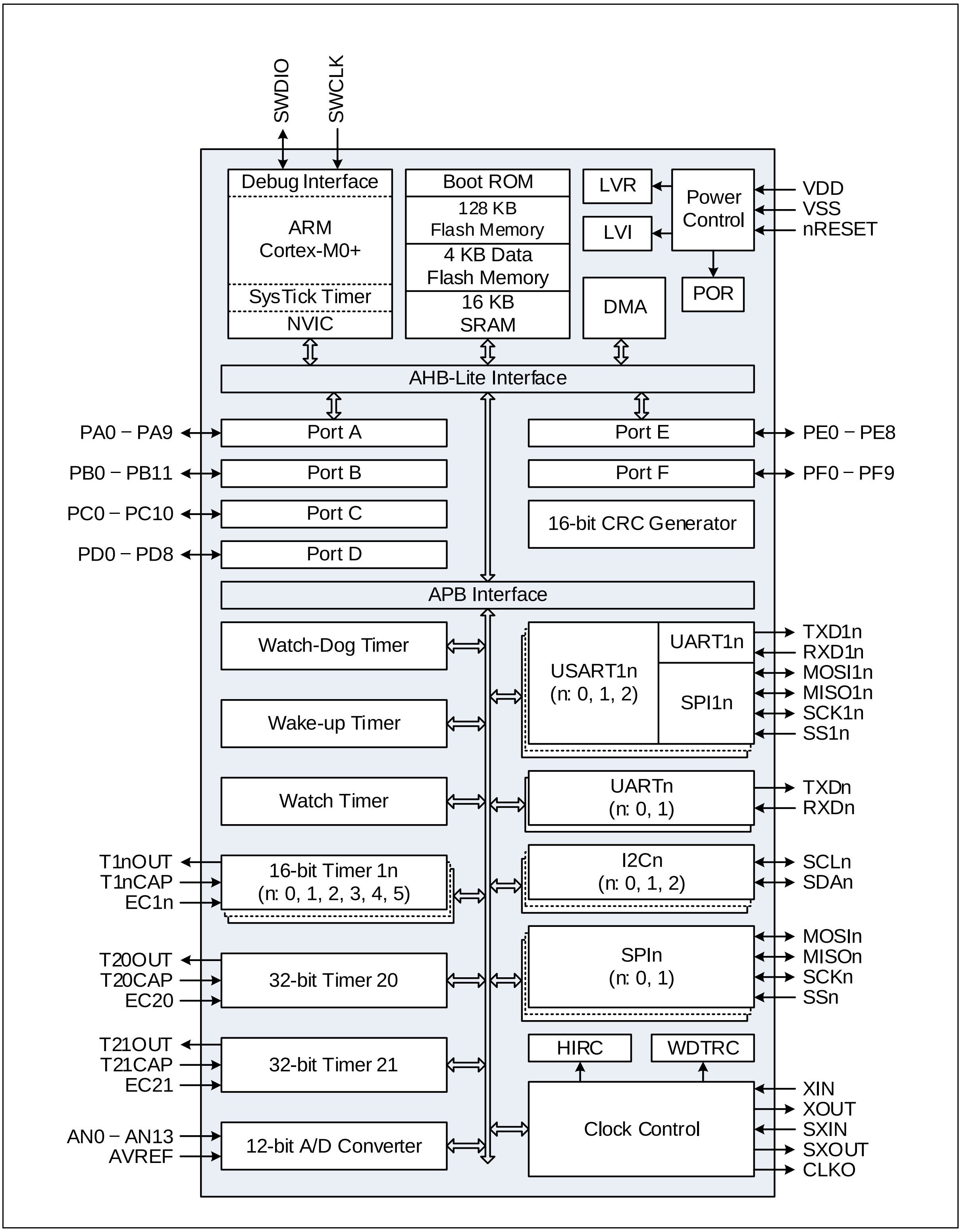
Table 4. Summary of A31S134 Peripherals

Peripheral		A31S134RL	A31S134CL	A31S134SN	A31S134KN A31S134KU
Memory	Code Flash	128 KB	128 KB	128 KB	128 KB
	Data Flash	4 KB	4 KB	4 KB	4 KB
	SRAM	16 KB	16 KB	16 KB	16 KB
Timers	General-Purpose	8	8	8	8
	SysTick	1	1	1	1
	WatchDog	1	1	1	1
	Watch	1	1	1	1
Communication Interfaces	USART	3	3	3	3
	UART	2	2	2	1
	I2C	3	3	3	2
	SPI	2	2	2	2
Direct Memory Access (DMA)		2	2	2	2
GPIO		61	45	41	29
ADC Number of channels		50 ksps	50 ksps	50 ksps	50 ksps
		14	14	14	8
Max. Operating Frequency		32 MHz	32 MHz	32 MHz	32 MHz
CRC		1	1	1	1
Operating Voltage		1.8 V to 5.5 V			
Operating Temperature	Commercial	−40°C to 85°C			
	Industrial	−40°C to 105°C			
Package		64-LQFP-1010	48-LQFP-0707	44-LQFP-1010	32-LQFP-0707 32-QFN-0505

2.3 Block Diagram

Figure 1 shows a block diagram of the A31S134.

Figure 1. A31S134 Block Diagram



2.4 Functional Overview

The following sections provide overviews of the features of the A31S134 microcontroller.

2.4.1 Cortex-M0+ Core

The A31S134 microcontroller uses the energy efficient Cortex-M0+ CPU core from Arm, which is optimized for low-power consumption and features a highly efficient 32-bit architecture. The Cortex-M0+ is based on the ARMv6-M Thumb instruction set and includes 16-bit instructions with Thumb-2 technology, allowing for improved performance and energy efficiency. It also includes a simple 24-bit system timer (SYSTICK) that can function as a real-time operating system or a counter. Additionally, the Cortex-M0+ features an integrated Nested Vectored Interrupt Controller (NVIC) for deterministic interrupt handling, hardware single-cycle multiplication for efficient computation, and supports SWD debugging features.

Refer to the technical reference manual **ARM DDI 0484C** for detailed information on Cortex-M0+.

2.4.2 On-chip SRAM

The A31S134 has a block of zero-wait on-chip SRAM. The size of the SRAM is 16 KB, and its base address is 0x2000_0000. The SRAM memory area is commonly utilized for storing data and as a stack memory. Additionally, it can also be utilized for storing program code for faster execution or during flash erasing and programming operations.

2.4.3 Operating Voltage

The device operates with a supply voltage of a 1.8 V to 5.5 V (VDD).

During a power-up process, a reset plays an important role and affects the entire process of the system booting. The A31S134 has two power-related reset options as described below:

- POR_RST (Power-On Reset): Controls the voltage less than 1.2 V.
- LVR_RST (Low-Voltage Reset): Controls the voltage less than 1.62 V (configuration option).

If the power level is higher than the POR and lower than the flash operating voltage (Min. 1.35 V), the Code Read operation may malfunction. To prevent this abnormal Code Read operation, the LVR_RST generates the **nSYSRESET** internal signal, and the microcontroller enters the reset mode to prevent the abnormal operation. To ensure stable operation, it is recommended to select a voltage level higher than the minimum level of 1.62 V that can be set by the LVR.

2.4.4 Operation Mode

2.4.4.1 Transition of Operation Mode

The INIT mode is the initial state of the chip when a reset is asserted. In the RUN mode, the CPU operates at the maximum performance with the high-speed clock system. The SLEEP and DEEP-SLEEP modes are available as low-power consumption modes. During these modes, the processor core and any unused peripherals are halted to effectively manage power consumption.

2.4.4.2 RUN Mode

In the RUN mode, the CPU and peripheral hardware operate with a high-speed clock. After a reset, the system will enter the RUN mode if the INIT state is detected.

2.4.4.3 SLEEP Mode

When the microcontroller enters the SLEEP mode, the CPU is halted while peripheral functions remain active. Users can determine which peripherals are active or inactive in the SLEEP mode by setting the corresponding function enable bit and clock enable bit in the SCU_PPCLKEN register.

2.4.4.4 DEEP-SLEEP Mode

In the DEEP-SLEEP mode, both the CPU and the system clock (MCLK) are halted to reduce power consumption. However, the Watch timer with a sub-clock and the watchdog timer with WDTRC can still operate in this mode.

2.4.4.5 Reset Mode

The A31S134 has two system reset options: a cold reset, which is effective during power up or down sequences, and a warm reset, which is triggered by multiple reset sources.

The reset features of the A31S134 are as follows:

- nRESET pin
- WatchDog Timer (WDT) reset
- Low-Voltage Reset (LVR)
- Monitor (MON) reset
- Software reset
- CPU request reset

2.4.5 Clocks and Startup

The A31S134 has two main operating clocks: HCLK, which generates clock signals for the CPU and AHB system, and PCLK, which generates clock signals for peripheral systems.

2.4.5.1 HCLK Clock

The Cortex-M0+ CPU requires two clocks: HCLK and FCLK. While the HCLK supplies the clock for both the CPU and AHB, the FCLK remains enabled unless the system enters the DEEP-SLEEP mode. Conversely, during the SLEEP mode, the HCLK can be disabled while the FCLK continues to function.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 32 MHz, the HCLK frequency must not exceed 32 MHz.

2.4.5.2 PCLK Clock

The PCLK can be used as a clock source for any peripheral. The SCU_PPCLKEN registers determine whether the PCLK is enabled or disabled for each peripheral. If a peripheral block's PCLK input is not enabled, its registers cannot be read. Additionally, it is important to note that the PCLK stops operating in the DEEP-SLEEP mode.

2.4.5.3 Clock Configuration Procedure

Initially, after power on, the HIRC (2 MHz) is enabled as a system clock source by default in the system operation sequence. The HIRC operates as a system clock until users configure other clock sources according to their needs.

To enable the XMOSC and XSOSC clocks, users can set the XMOSCEN and XSOSCEN bits in the SCU_CLKSRCR register. However, before enabling the XMOSC and XSOSC blocks, users must first configure the pin mux settings for the XIN/XOUT and SXIN/SXOUT functions. Note that PF5/PF6 and PF3/PF4 pins are shared between these functions, and thus the PF_MOD and PF_AFSR1 registers must be configured correctly.

Once the XMOSC and XSOSC clocks are enabled, users can verify the stability of the crystal oscillation by using the clock monitoring control register, SCU_CMONCR. However, it is important to wait at least 10 ms to ensure that the crystal oscillation is stable before changing the system clock.

2.4.6 Nested Vectored Interrupt Controller (NVIC)

The A31S134 incorporates the Nested Vector Interrupt Controller (NVIC), which can manage up to 32 maskable interrupt channels with four priority levels. The NVIC in the Cortex-M0+ processor handles and prioritizes interrupts internally within the processor. Software can set the priority of each interrupt, and external interrupt signals are connected to the NVIC, which prioritizes them. The NVIC enables efficient processing of late-arriving interrupts and achieves low-latency interrupt processing. Access to all NVIC registers is only possible through word transfers.

The NVIC has the following advantages:

- Interrupt processing with reduced interrupt latency
- Direct transfer of Interrupt Vector Table (IVT) address to the core
- Fast interrupt processing capability
- Nested interrupt processing by priority: Interrupts with higher priority are given precedence over those with lower priority, even if they occur after the lower-priority interrupts.
- Tail Chaining interrupt processing.
- Automatically saves processor(core) state when interrupts are entered.
- Interrupt restoring without instructional overhead at the end of the interrupt

The NVIC hardware block provides flexible and efficient interrupt management with minimal interrupt latency.

2.4.7 Port Control Unit (PCU)

The A31S134 has a Port Control Unit (PCU) module that controls the input and output (I/O) ports. By setting the PCU registers, users can configure the functionality, input / output direction, pull-up / pull-down, and debouncing of the pins for their applications.

2.4.8 General-Purpose Input/Output (GPIO)

Pins other than those specified as VDD, GND or certain purpose, can be used as General-Purpose Input/Output (GPIO) pins.

The GPIO module controls the general I/O pins. Output pins can be configured to output high-level or low-level signals by setting the corresponding bits of the GPIO control register. On the other hand, the input status of logic input pins can be monitored through the control registers.

2.4.9 Embedded Flash Memory

The flash memory controller serves as an interface between the core and the embedded flash memory and is responsible for managing the data stored on the flash memory.

The flash memory of the A31S134 has the following features:

- Code flash memory for 128 KB with write protection bits
- Erase units
  - Page (256-byte)
  - Bulk (128 KB, full-chip)
- Program unit:
  - Word (4-byte)
  - Page (256-byte)
- Code flash read protection

2.4.10 Embedded Data Flash Memory

The data flash memory controller is an interface controller for embedded data flash memory. It manages data stored on the data flash memory.

The data flash memory of the A31S134 has the following features:

- Data flash memory for 4 KB with write protection bits
- Erase units
  - Page (32-byte)
  - Bulk (4 KB)
- Program unit
  - Word (4-byte)
  - Page (32-byte)

2.4.11 Direct Memory Access (DMA) Controller

The Direct Memory Access (DMA) controller is used for high-speed data transfers between peripherals and memories. The DMA allows quick data transfers by copying or moving data between memory and peripherals, without involving the core.

- Two channels of direct memory access
- 8-/ 16- / 32-bit data transfers
- Memory to peripheral transmission
- Peripheral to memory transmission
- DMA transfers are triggered by peripheral interrupts

2.4.12 16-bit and 32-bit Timers

The A31S134 includes six 16-bit and two 32-bit Timers that offer four operating modes: Periodic Mode, PWM Mode, One-shot Mode, and Capture Mode.

Users can select an input clock source for the 16-bit and 32-bit Timers, either a divided PCLK or an external clock. Especially for the 32-bit timer 20, XSOSC can be selected as an input clock source. An internal 12-bit prescaler allows to generate a variety of base clocks for the timers.

When the timer operates in Periodic Mode, interrupts can be triggered at regular intervals. In PWM Mode, users can set the period and duty to generate a PWM signal. In One-shot mode, the timer can generate one PWM waveform. In Capture Mode, the timer can measure pulse intervals of an external input signal based on the predefined conditions. In addition, the timer can transmit signals to control other devices, and is primarily used as a periodic tick timer or as a wake-up source.

2.4.13 WatchDog Timer (WDT)

The Watchdog Timer (WDT) is used to detect errors in the microcontroller caused by external interference or unexpected logical conditions. These errors cause the application program to deviate from its normal sequence. If the microcontroller loses control, the WDT will reset the microcontroller, allowing it to return to normal operation.

The WDT of the A31S134 is a 24-bit down counter. If the WDT is set as a reset source, the microcontroller restarts when the down counter reaches zero.

When it is not used to monitor the microcontroller, the WDT can be used as a cycle timer along with an interrupt.

2.4.14 Watch Timer (WT)

The Watch Timer (WT) can be used as a Real Time Clock (RTC) and is commonly used in RTC designs. Its internal structure includes a clock source select circuit, a timer counter circuit, an output select circuit, and a watch timer control register. To operate the WT, select the input clock source and output interval, and set the WTEN bit to 1 in the WT control register (WT_CR). The WT can be operated individually or simultaneously with other functions. To stop the WT, clear the WTEN bit in the WT_CR register. Even when the CPU is in deep sleep mode, the sub-clock remains active, and the WT continues to operate. The WT_CR can be used to clear and set the WT interval value when writing, and to read the 12-bit WT counter value. The key features of the WT are as follows:

- 14-bit divider
- 12-bit up-counter
- RTC functionality

2.4.15 Universal Synchronous and Asynchronous Receiver Transmitter (USART)

The A31S134 has a three-channel USART module. The USART module supports UART and SPI modes and features as follows:

- Full duplex operation with independent serial receive and transmit registers
- Asynchronous or synchronous communication
- Baud rate generator
- Supports serial frames with 5- to 9-bit data transfer length and 1 or 2 stop bits generation and checking
- Even / Odd / Non-parity generation and checking-
- Receive character (data) detection and receive time-out function
- Local Interconnection Network (LIN)
- Data over-run detection
- Framing error detection
- Supports three types of interrupts: TX completion, TX data register empty and RX completion
- Double speed asynchronous communication mode
- Up to 8 MHz data transfer in SPI mode

2.4.16 Universal Asynchronous Receiver Transmitter (UART)

The A31S134 has a two-channel UART module. The built-in UART module allows users to specify settings for transmitting and receiving data and provides the ability to read the status of the UART. By providing information about the current state of transmission and reception processes, including types and conditions, the UART module enables users to monitor for potential errors such as parity, overrun, framing, or break interrupts during data reception.

The UART module includes a programmable baud rate generator for each channel, which generates an internal 16x clock for sampling of the UART unit by dividing a prescaled clock using a baud rate divisor that ranges from 0 to 65,535.

Users can program interrupts that can control the UART communication.

Furthermore, the built-in DMA allows the UART module to transfer data directly to or from memory without involving the CPU, reducing CPU usage, and increasing the speed of data transfer.

2.4.17 Serial Peripheral Interface (SPI)

The A31S134 has two built-in Serial Peripheral Interface (SPI) modules, which are clock-synchronized, and allow for customizable transmission clock specifications.

The SPI modules facilitate communications between one master and multiple slaves, which can be chosen using the Slave Select (SS) signal. Using four signal terminals (SS, SCK, MOSI, and MISO), the SPI module enables three or four-wire synchronous transfers. Its Transmit and Receive Buffers are separate, which enables full-duplex communication and simultaneous reading and writing of data.

2.4.18 Inter-Integrated Circuit (I2C) Interface

The Inter-Integrated Circuit (I2C) interface built in the A31S134 is compliant with the standard I2C communication protocol. It is used for serial communication between internal and external devices via the I2C protocol.

The built-in I2C interface, equipped with three units, supports both master and slave modes, and can transmit and receive data in bytes by using interrupts or polling.

The I2C of the A31S134 operates in Standard mode (100 kHz), Fast mode (400 kHz) or Fast Plus mode (1 MHz). In addition, it also supports General call.

The I2C interface facilitates communication with multiple peripherals that share the same bus type. To utilize I2C, it is recommended to configure the SCL and SDA pins as open-drain and attach external pull-up resistors to ensure that their output signals are maintained at the high-level.

Table 5. Features of I2Cn (n = 0 to 2)

I2C Features	I2C0	I2C1	I2C2
7-bit addressing mode	O	O	O
Standard mode (up to 100 kbit/s)	O	O	O
Fast mode (up to 400 kbit/s)	O	O	O
Fast Plus mode (up to 1,000 kbit/s)	O	O	O
General call	O	O	O

2.4.19 Analog-to-Digital Converter (ADC)

The A31S134 is equipped with a 12-bit Analog-to-Digital Converter (ADC) module that supports up to 14 analog inputs. The module includes three registers: a control register (ADC_CR), a data register (ADC_DR), and a prescaler data register (ADC_PREDR). To select channels for conversion, users can set the ADSEL[3:0] bit in the ADC_CR register. Once conversion is completed, the result is loaded into the ADC_DR register and the A/D conversion status bit (ADCIFLAG) is set to '1', triggering an A/D interrupt. The ADCIFLAG bit is read as 0 during A/D conversion.

The main features of the ADC are as follows:

- 14-channel analog inputs
- Supports for software start (ADST) and timer trigger (T10/11/12 A match)
- Conversion time of 58 clocks
- 5-bit prescaler

2.4.20 Cyclic Redundancy Check (CRC) Calculation Module

The A31S134 has a built-in Cyclic Redundancy Check (CRC) module capable of computing 16-bit CRC codes from data streams and flash memories. CRC-based techniques are commonly used to ensure the integrity of data transmission or storage and can also be used to verify the integrity of flash memory in compliance with functional safety standards. By computing a signature of the software during runtime and comparing it with a reference signature, the CRC module can help detect any changes made to the software.

The CRC module in the A31S134 offers the following features:

- Auto CRC and user CRC mode
- Supports CRC-CCITT ($G1(x) = x^{16} + x^{12} + x^5 + 1$)
- Supports CRC-16 ($G2(x) = x^{16} + x^{15} + x^2 + 1$)
- CRC and checksum mode
- CRC/checksum start address auto increment (user mode only)

2.5 Development Tools

In this chapter, various development tools for the A31S134 are described. ABOV provides software tools, debuggers, and programmers to assist users in achieving the desired results for their target applications. ABOV supports the development ecosystem for our customers.

2.5.1 Compiler

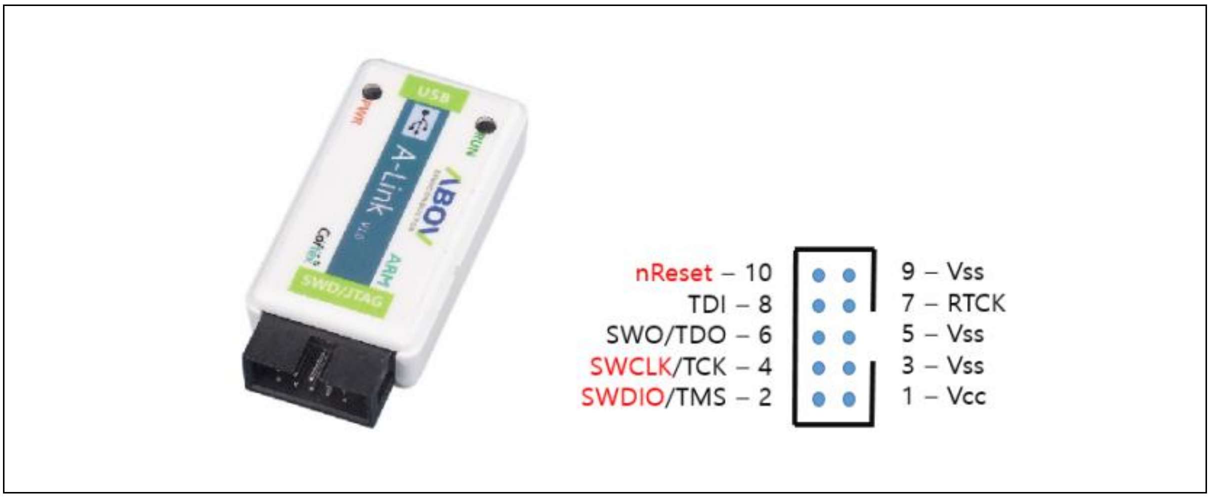
Since the A31S134 has the Arm 32-bit Cortex-M0+ core, any third-party compiler, such as Keil, IAR and GCC cross-C compiler supporting Cortex-M0+, is available.

2.5.2 Debugger

A-Link and A-LinkPro can be used to emulate the A31S134 microcontroller using the SWD interface and have a two-wire interface to connect to the microcontroller on the user system. A-Link and A-LinkPro provide extensive debugging capabilities for the micrcontroller, including the ability to read or write the value of the microcontroller's internal memory and I/O peripherals, as well as control its internal debugging logic. A-Link and A-LinkPro are debug interfaces with third-party compilers, providing an excellent combination of debugging environments.

The figure below shows the pinout for programming with the A-Link and A-LinkPro. For more detailed information about the A-Link and A-LinkPro, please visit www.abovsemi.com and download related software and documents.

Figure 2. A-Link and Pin Description



2.5.3 Programmer

2.5.3.1 E-PGM+ and E-PGM Serial

E-PGM+ and E-PGM Serial are standalone programmers, which allow users to program directly on the device.

- Supports for all ABOV microcontroller devices
- Dedicated tool for mass production
- 40-pin Textool DIP socket for single chip programming (E-PGM+ only)
- 10-pin connector for ISP mode
- USB host interface
- HEX downloads and controls

2.5.3.2 Gang Programmer

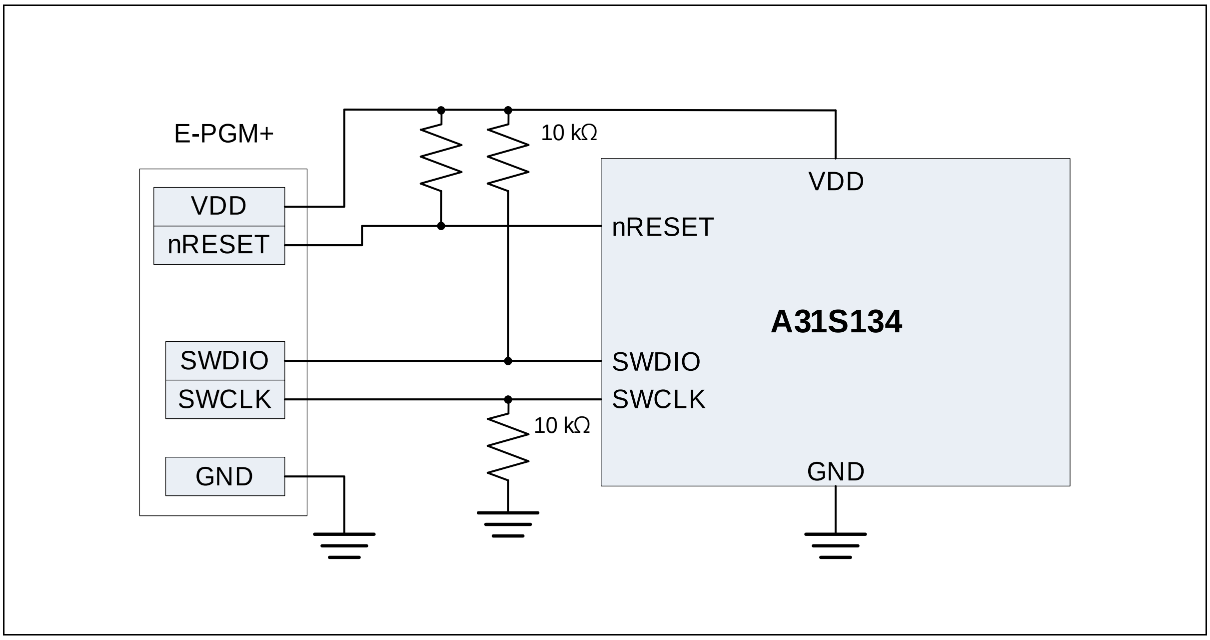
E-Gang4 and E-Gang6 can program multiple devices simultaneously and operate in host-controlled and standalone modes without requiring a host computer connection. These programmers feature a USB interface for easy connection to a handler.

NOTE: Refer to ABOV homepage "Tools & Support > Programmer".

2.5.3.3 SWD Mode and E-PGM+ Connections

The connection between the A31S134 and E-PGM+ using the SWD interface is illustrated in Figure 3.

Figure 3. Connection between A31S134 and E-PGM+ using SWD Interface



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3. Pinouts and Pin Descriptions

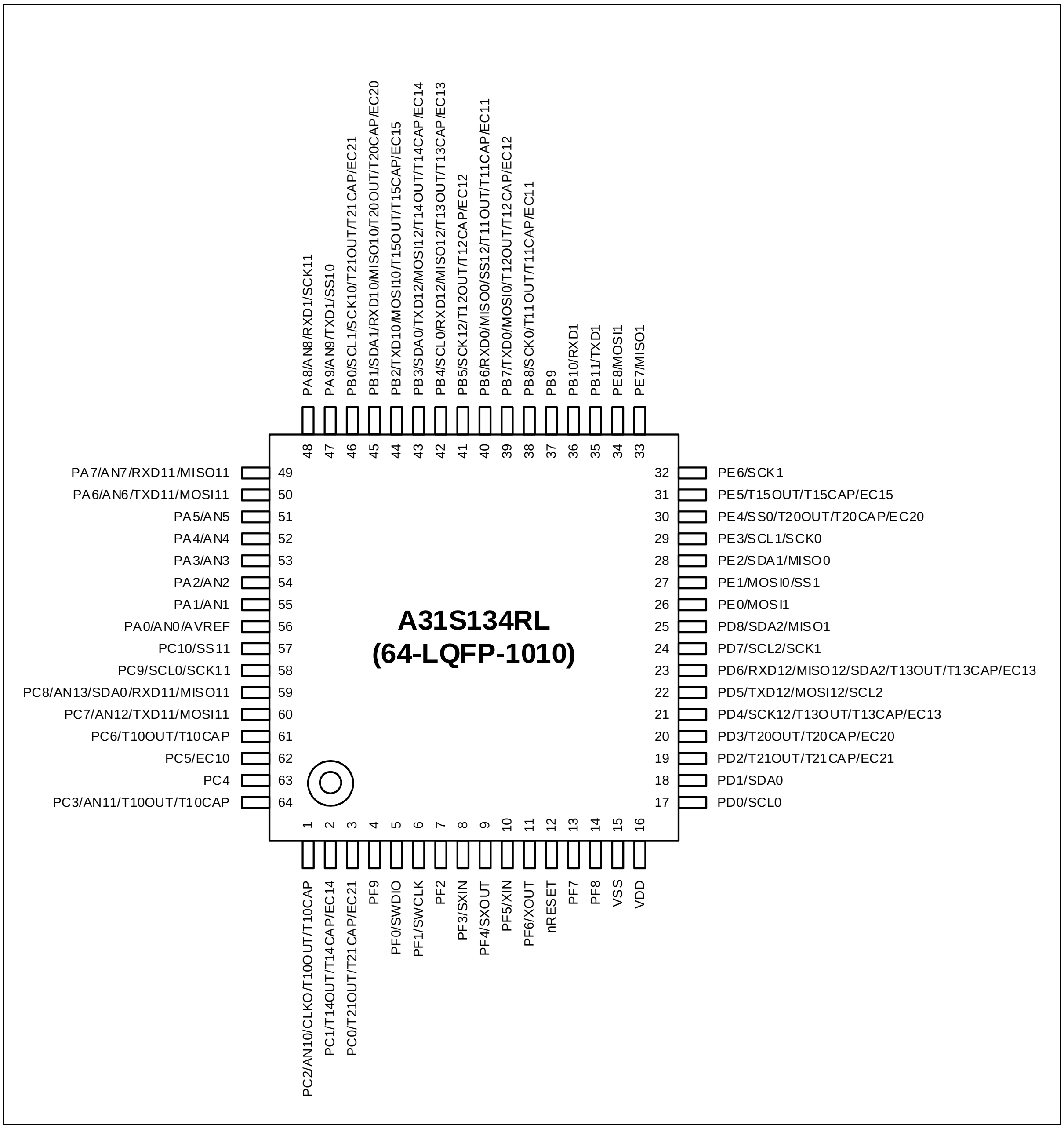
In this chapter, pinouts and pin descriptions of the A31S134 are described.

3.1 Pinouts

Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 show the top view of the packages.

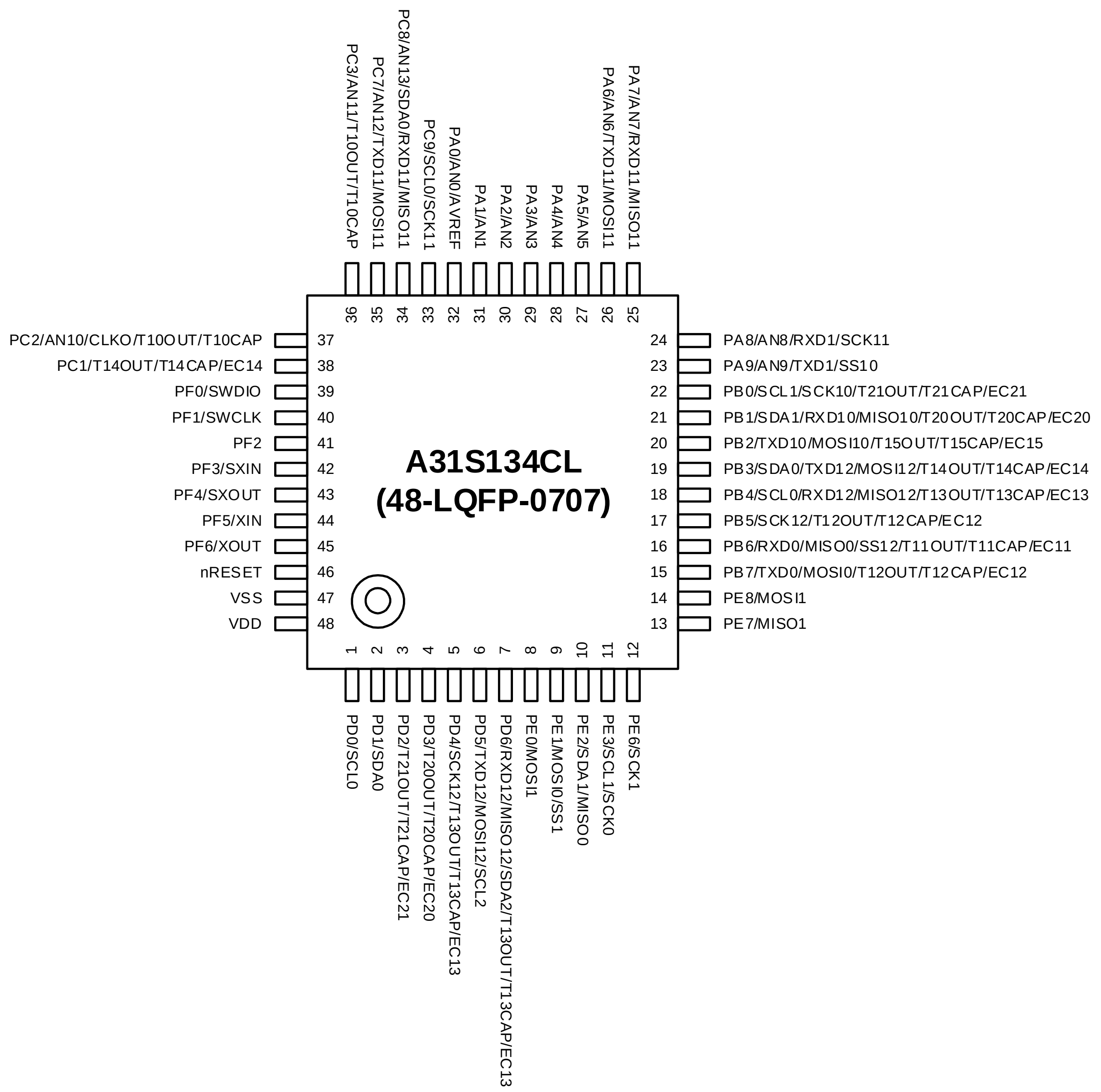
3.1.1 A31S134RL (64-LQFP)

Figure 4. 64-LQFP Pinouts



3.1.2 A31S134CL (48-LQFP)

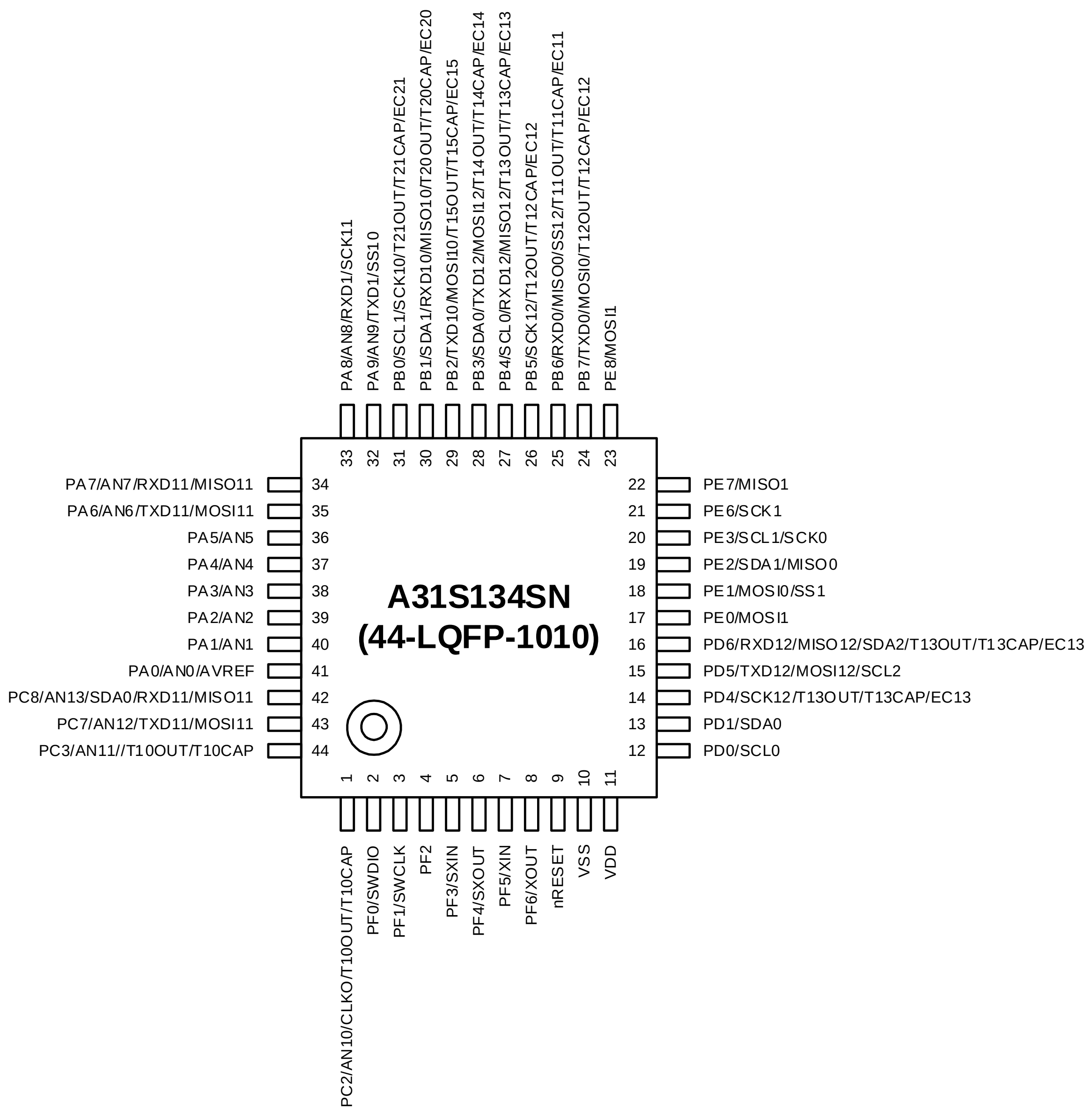
Figure 5. 48-LQFP Pinouts



NOTE: When using the 48-LQFP package, each of the PB[11:8], PC[10, 6:4, 0], PD[8:7], PE[5:4], and PF[9:7] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.3 A31S134SN (44-LQFP)

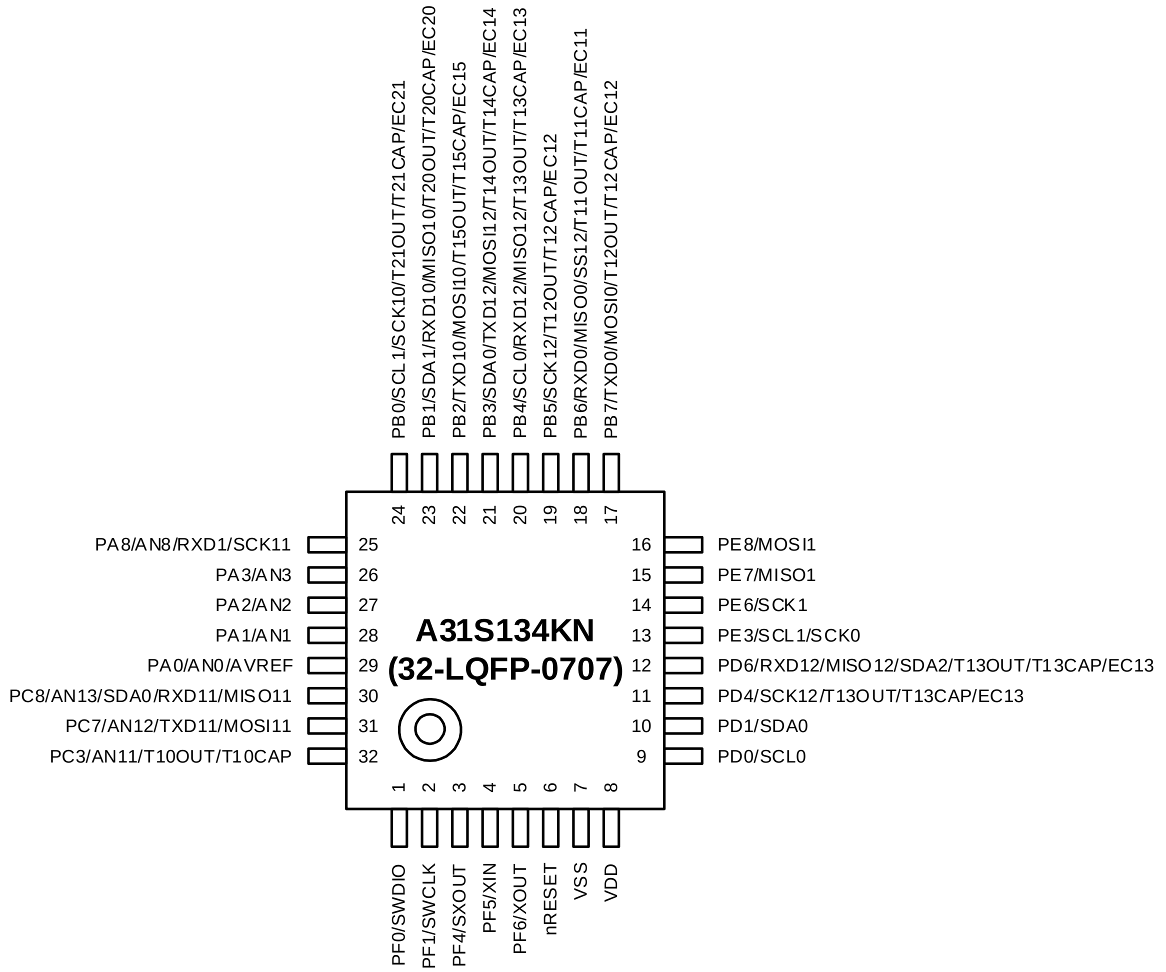
Figure 6. 44-LQFP Pinouts



NOTE: When using the 44-LQFP package, each of the PB[11:8], PC[10:9, 6:4, 1:0], PD[8:7, 3:2], PE[5:4], and PF[9:7] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.4 A31S134KN (32-LQFP)

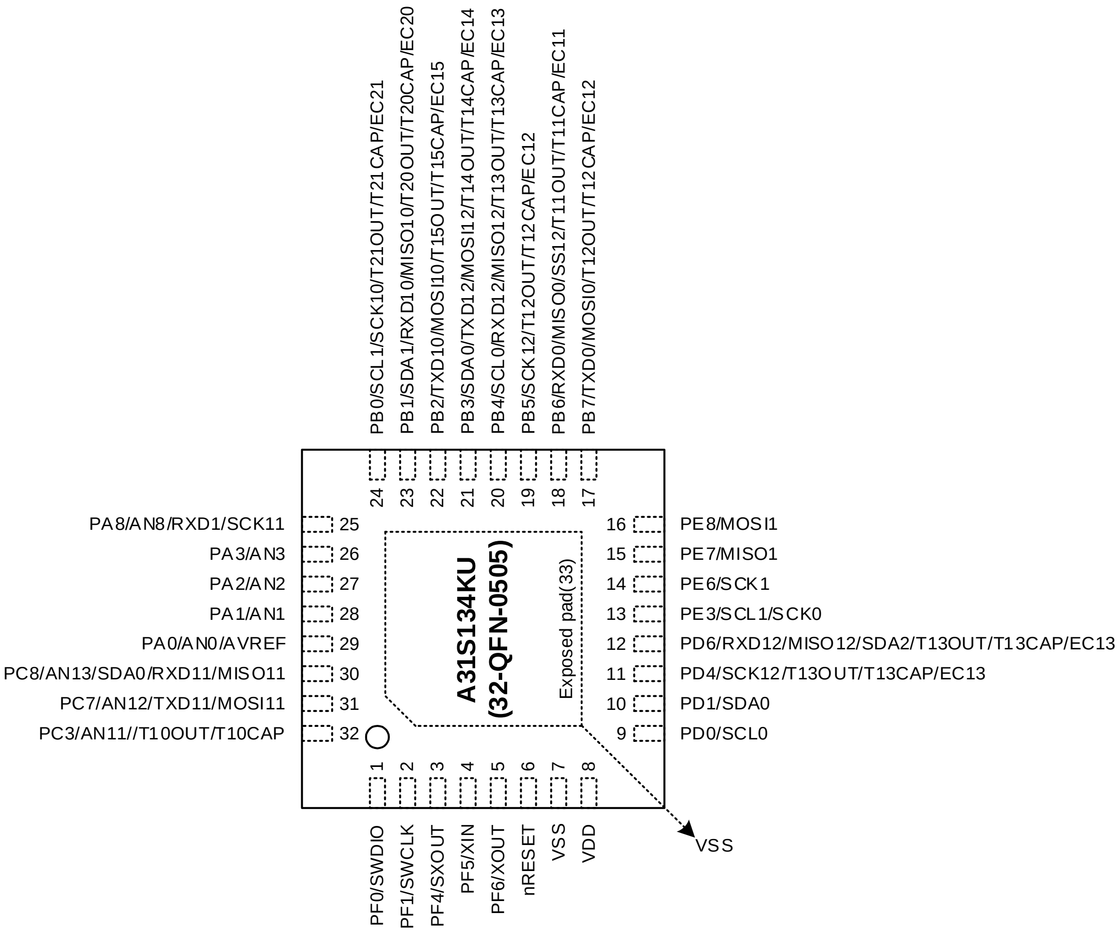
Figure 7. 32-LQFP Pinouts



NOTE: When using the 32-LQFP package, each of the PA[9, 7:4], PB[11:8], PC[10:9, 6:4, 2:0], PD[8:7, 5, 3:2], PE[5:4, 2:0], and PF[9:7, 3:2] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.1.5 A31S134KU (32-QFN)

Figure 8. 32-QFN Pinouts



NOTE: When using the 32-QFN package, each of the PA[9, 7:4], PB[11:8], PC[10:9, 6:4, 2:0], PD[8:7, 5, 3:2], PE[5:4, 2:0], and PF[9:7, 3:2] pins should be configured as either a push-pull output or an input with a pull-up or pull-down resistor by software control using the appropriate registers or configuration settings.

3.2 Pin Description

Table 6. Legend and Abbreviation used in Pin Description

Name	Abbreviation	Definition
Pin Name	The function of the pin.	
Pin Type	I	Input
	O	Output
	I/O	Input/Output
	U	Pull-up
	D	Pull-down
	S	Schmitt-Trigger input
	C	CMOS input
	A	Analog
	P	Power

NOTES:

1. After a reset, all the pins are configured to function defined by their initial values. The initial value of the pin depends on the reset value. This configuration follows the 64-pin standard.
2. Do not configure unused pins as floating inputs.
3. After a reset, the alternate functions of the PF0 and PF1 pins are set as SWDIO and SWCLK, respectively, and the internal pull-down on SWCLK and the internal pull-up on SWDIO are enabled.
4. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.

Pin configuration information in Table 7 contains one pair of power/ground and other dedicated pins. These multi-function pins have up to six selections of functions including GPIO.

Table 7. Pin Description

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin				
1	37	1	–	PC2(1)	IOUDS	Port C bit 2 input / output	
				AN10	IA	A/D converter analog input channel	
				CLKO	O	System clock output	
				T10OUT	O	Timer 10 pulse output	
				T10CAP	I	Timer 10 capture input	
2	38	–	–	PC1(1)	IOUDS	Port C bit 1 input / output	
				T14OUT	O	Timer 14 pulse output	
				T14CAP	I	Timer 14 capture input	
				EC14	I	Timer 14 event count input	
3	–	–	–	PC0(1)	IOUDS	Port C bit 0 input / output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				EC21	I	Timer 21 event count input	
4	–	–	–	PF9(1)	IOUDS	Port F bit 9 input / output	
5	39	2	1	PF0(1)	IOUDS	Port F bit 0 input / output	
				SWDIO(1)(3)(4)	I/O	SWD data input / output	Pull-up when reset
6	40	3	2	PF1(1)	IOUDS	Port F bit 1 input / output	
				SWCLK(1)(3)(4)	I	SWD clock input	Pull-down when reset
7	41	4	–	PF2(1)	IOUDS	Port F bit 2 input / output	
8	42	5	–	PF3(1)	IOUDS	Port F bit 3 input / output	
				SXIN	IA	Sub-oscillator input	
9	43	6	3	PF4(1)	IOUDS	Port F bit 4 input / output	
				SXOUT	OA	Sub-oscillator output	
10	44	7	4	PF5(1)	IOUDS	Port F bit 5 input / output	
				XIN	IA	Main oscillator input	
11	45	8	5	PF6(1)	IOUDS	Port F bit 6 input / output	
				XOUT	OA	Main oscillator output	
12	46	9	6	nRESET	IU	External reset input	Always pull-up
13	–	–	–	PF7(1)	IOUDS	Port F bit 7 input / output	
14	–	–	–	PF8(1)	IOUDS	Port F bit 8 input / output	
15	47	10	7	VSS	P	Ground	
16	48	11	8	VDD	P	VDD	
17	1	12	9	PD0(1)	IOUDS	Port D bit 0 input / output	
				SCL0	IO	I2C clock input / output	
18	2	13	10	PD1(1)	IOUDS	Port D bit 1 input / output	
				SDA0	IO	I2C data input / output	
19	3	–	–	PD2(1)	IOUDS	Port D bit 2 input / output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				EC21	I	Timer 21 event count input	

Table 7. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin				
20	4	–	–	PD3(1)	IOUDS	Port D bit 3 input / output	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				EC20	I	Timer 20 event count input	
21	5	14	11	PD4(1)	IOUDS	Port D bit 4 input / output	
				SCK12	IO	SPI clock input / output	
				T13OUT	O	Timer 13 pulse output	
				T13CAP	I	Timer 13 capture input	
				EC13	I	Timer 13 event count input	
22	6	15	–	PD5(1)	IOUDS	Port D bit 5 input / output	
				SCL2	IO	I2C clock input/output	
				TXD12	O	UART data output	
				MOSI12	IO	SPI master out slave in	
23	7	16	12	PD6(1)	IOUDS	Port D bit 6 input / output	
				SDA2	IO	I2C data input / output	
				RXD12	I	UART data input	
				MISO12	IO	SPI master in slave out	
				T13OUT	O	Timer 13 pulse output	
				T13CAP	I	Timer 13 capture input	
				EC13	I	Timer 13 event count input	
24	–	–	–	PD7(1)	IOUDS	Port D bit 7 input / output	
				SCL2	IO	I2C clock input / output	
				SCK1	IO	SPI clock input / output	
25	–	–	–	PD8(1)	IOUDS	Port D bit 8 input / output	
				SDA2	IO	I2C data input / output	
				MISO1	IO	SPI master in slave out	
26	8	17	–	PE0(1)	IOUDS	Port E bit 0 input / output	
				MOSI1	IO	SPI master out slave in	
27	9	18	–	PE1(1)	IOUDS	Port E bit 1 input / output	
				MOSI0	IO	SPI master out slave in	
				SS1	I	SPI slave select input	
28	10	19	–	PE2(1)	IOUDS	Port E bit 2 input / output	
				SDA1	IO	I2C data input / output	
				MISO0	IO	SPI master in slave out	
29	11	20	13	PE3(1)	IOUDS	Port E bit 3 input / output	
				SCL1	IO	I2C clock input / output	
				SCK0	IO	SPI clock input / output	
30	–	–	–	PE4(1)	IOUDS	Port E bit 4 input / output	
				SS0	I	SPI slave select input	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				EC20	I	Timer 20 event count input	

Table 7. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin				
31	–	–	–	PE5(1)	IOUDS	Port E bit 5 input / output	
				T15OUT	O	Timer 15 pulse output	
				T15CAP	I	Timer 15 capture input	
				EC15	I	Timer 15 event count input	
32	12	21	14	PE6(1)	IOUDS	Port E bit 6 input / output	
				SCK1	IO	SPI clock input/output	
33	13	22	15	PE7(1)	IOUDS	Port E bit 7 input / output	
				MISO1	IO	SPI master in slave out	
34	14	23	16	PE8(1)	IOUDS	Port E bit 8 input / output	
				MOSI1	IO	SPI master out slave in	
35	–	–	–	PB11(1)	IOUDS	Port B bit 11 input / output	
				TXD1	O	UART data output	
36	–	–	–	PB10(1)	IOUDS	Port B bit 10 input / output	
				RXD1	I	UART data input	
37	–	–	–	PB9(1)	IOUDS	Port B bit 9 input / output	
38	–	–	–	PB8(1)	IOUDS	Port B bit 8 input / output	
				SCK0	IO	SPI clock input / output	
				T11OUT	O	Timer 11 pulse output	
				T11CAP	I	Timer 11 capture input	
				EC11	I	Timer 11 event count input	
39	15	24	17	PB7(1)	IOUDS	Port B bit 7 input / output	
				TXD0	O	UART data output	
				MOSI0	IO	SPI master out slave in	
				T12OUT	O	Timer 12 pulse output	
				T12CAP	I	Timer 12 capture input	
				EC12	I	Timer 12 event count input	
40	16	25	18	PB6(1)	IOUDS	Port B bit 6 input / output	
				RXD0	I	UART data input	
				MISO0	IO	SPI master in slave out	
				SS12	I	SPI slave select input	
				T11OUT	O	Timer 11 pulse output	
				T11CAP	I	Timer 11 capture input	
				EC11	I	Timer 11 event count input	
41	17	26	19	PB5(1)	IOUDS	Port B bit 5 input / output	
				SCK12	IO	SPI clock input / output	
				T12OUT	O	Timer 12 pulse output	
				T12CAP	I	Timer 12 capture input	
				EC12	I	Timer 12 event count input	
42	18	27	20	PB4(1)	IOUDS	Port B bit 4 input / output	
				SCL0	IO	I2C clock input / output	
				RXD12	I	UART data input	
				MISO12	IO	SPI master in slave out	
				T13OUT	O	Timer 13 pulse output	
				T13CAP	I	Timer 13 capture input	
				EC13	I	Timer 13 event count input	

Table 7. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin				
43	19	28	21	PB3(1)	IOUDS	Port B bit 3 input / output	
				SDA0	IO	I2C data input / output	
				TXD12	O	UART data output	
				MOSI12	IO	SPI master out slave in	
				T14OUT	O	Timer 14 pulse output	
				T14CAP	I	Timer 14 capture input	
				EC14	I	Timer 14 event count input	
44	20	29	22	PB2(1)	IOUDS	Port B bit 2 input / output	
				TXD10	O	UART data output	
				MOSI10	IO	SPI master out slave in	
				T15OUT	O	Timer 15 pulse output	
				T15CAP	I	Timer 15 capture input	
				EC15	I	Timer 15 event count input	
45	21	30	23	PB1(1)	IOUDS	Port B bit 1 input / output	
				SDA1	IO	I2C data input / output	
				RXD10	I	UART data input	
				MISO10	IO	SPI master in slave out	
				T20OUT	O	Timer 20 pulse output	
				T20CAP	I	Timer 20 capture input	
				EC20	I	Timer 20 event count input	
46	22	31	24	PB0(1)	IOUDS	Port B bit 0 input / output	
				SCL1	IO	I2C clock input / output	
				SCK10	IO	SPI clock input / output	
				T21OUT	O	Timer 21 pulse output	
				T21CAP	I	Timer 21 capture input	
				EC21	I	Timer 21 event count input	
47	23	32	–	PA9(1)	IOUDS	Port A bit 9 input / output	
				AN9	IA	A/D converter analog input channel	
				SS10	I	SPI slave select input	
				TXD1	O	UART data output	
48	24	33	25	PA8(1)	IOUDS	Port A bit 8 input / output	
				AN8	IA	A/D converter analog input channel	
				SCK11	IO	SPI clock input / output	
				RXD1	I	UART data input	
49	25	34	–	PA7(1)	IOUDS	Port A bit 7 input / output	
				AN7	IA	A/D converter analog input channel	
				RXD11	I	UART data input	
				MISO11	IO	SPI master in slave out	

Table 7. Pin Description (continued)

Pin Number				Pin Name	Type	Description	Remark
64-pin	48-pin	44-pin	32-pin				
50	26	35	–	PA6(1)	IOUDS	Port A bit 6 input / output	
				AN6	IA	A/D converter analog input channel	
				TXD11	O	UART data output	
				MOSI11	IO	SPI master out slave in	
51	27	36	–	PA5(1)	IOUDS	Port A bit 5 input / output	
				AN5	IA	A/D converter analog input channel	
52	28	37	–	PA4(1)	IOUDS	Port A bit 4 input / output	
				AN4	IA	A/D converter analog input channel	
53	29	38	26	PA3(1)	IOUDS	Port A bit 3 input / output	
				AN3	IA	A/D converter analog input channel	
54	30	39	27	PA2(1)	IOUDS	Port A bit 2 input / output	
				AN2	IA	A/D converter analog input channel	
55	31	40	28	PA1(1)	IOUDS	Port A bit 1 input / output	
				AN1	IA	A/D converter analog input channel	
56	32	41	29	PA0(1)	IOUDS	Port A bit 0 input / output	
				AN0	IA	A/D converter analog input channel	
				AVREF	IA	A/D converter reference input	
57	–	–	–	PC10(1)	IOUDS	Port C bit 10 input / output	
				SS11	I	SPI slave select input	
58	33	–	–	PC9(1)	IOUDS	Port C bit 9 input / output	
				SCL0	IO	I2C clock input / output	
				SCK11	IO	SPI clock input / output	
59	34	42	30	PC8(1)	IOUDS	Port C bit 8 input / output	
				AN13	IA	A/D converter analog input channel	
				SDA0	IO	I2C data input / output	
				RXD11	I	UART data input	
				MISO11	IO	SPI master in slave out	
60	35	43	31	PC7(1)	IOUDS	Port C bit 7 input / output	
				AN12	IA	A/D converter analog input channel	
				TXD11	O	UART data output	
				MOSI11	IO	SPI master out slave in	
61	–	–	–	PC6(1)	IOUDS	Port C bit 6 input / output	
				T10OUT	O	Timer 10 pulse output	
				T10CAP	I	Timer 10 capture input	
62	–	–	–	PC5(1)	IOUDS	Port C bit 5 input / output	
				EC10	I	Timer 10 event count input	
63	–	–	–	PC4(1)	IOUDS	Port C bit 4 input / output	
64	36	44	32	PC3(1)	IOUDS	Port C bit 3 input / output	
				AN11	IA	A/D converter analog input channel	
				T10OUT	O	Timer 10 pulse output	
				T10CAP	I	Timer 10 capture input	

3.3 Alternate Function Pins

The GPIO pins have alternate functions as described in Table 8.

Table 8. GPIO Alternate Functions

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF5
PA0	AN0	AVREF	–	–	–	–
PA1	AN1	–	–	–	–	–
PA2	AN2	–	–	–	–	–
PA3	AN3	–	–	–	–	–
PA4	AN4	–	–	–	–	–
PA5	AN5	–	–	–	–	–
PA6	AN6	–	–	MOSI11	TXD11	–
PA7	AN7	–	–	MISO11	RXD11	–
PA8	AN8	–	–	SCK11	RXD1	–
PA9	AN9	–	–	–	TXD1	SS10
PB0	T21OUT	T21CAP	EC21	SCK10	–	SCL1
PB1	T20OUT	T20CAP	EC20	MISO10	RXD10	SDA1
PB2	T15OUT	T15CAP	EC15	MOSI10	TXD10	–
PB3	T14OUT	T14CAP	EC14	MOSI12	TXD12	SDA0
PB4	T13OUT	T13CAP	EC13	MISO12	RXD12	SCL0
PB5	T12OUT	T12CAP	EC12	SCK12	–	–
PB6	T11OUT	T11CAP	EC11	MISO0	RXD0	SS12
PB7	T12OUT	T12CAP	EC12	MOSI0	TXD0	–
PB8	T11OUT	T11CAP	EC11	SCK0	–	–
PB9	–	–	–	–	–	–
PB10	–	–	–	–	RXD1	–
PB11	–	–	–	–	TXD1	–
PC0	T21OUT	T21CAP	EC21	–	–	–
PC1	T14OUT	T14CAP	EC14	–	–	–
PC2	AN10	CLKO	–	T10OUT	T10CAP	–
PC3	AN11	–	–	T10OUT	T10CAP	–
PC4	–	–	–	–	–	–
PC5	–	–	EC10	–	–	–
PC6	T10OUT	T10CAP	–	–	–	–
PC7	AN12	–	–	MOSI11	TXD11	–
PC8	AN13	–	–	MISO11	RXD11	SDA0
PC9	–	–	–	SCK11	–	SCL0
PC10	–	–	–	SS11	–	–

Table 8. GPIO alternate functions (continued)

Pin Name	Alternate Function					
	AF0	AF1	AF2	AF3	AF4	AF5
PD0	–	–	–	–	–	SCL0
PD1	–	–	–	–	–	SDA0
PD2	T21OUT	T21CAP	EC21	–	–	–
PD3	T20OUT	T20CAP	EC20	–	–	–
PD4	T13OUT	T13CAP	EC13	SCK12	–	–
PD5	–	–	–	MOSI12	TXD12	SCL2
PD6	T13OUT	T13CAP	EC13	MISO12	RXD12	SDA2
PD7	–	–	–	SCK1	–	SCL2
PD8	–	–	–	MISO1	–	SDA2
PE0	–	–	–	MOSI1	–	–
PE1	–	–	–	MOSI0	–	SS1
PE2	–	–	–	MISO0	SDA1	–
PE3	–	–	–	SCK0	SCL1	–
PE4	T20OUT	T20CAP	EC20	–	–	SS0
PE5	T15OUT	T15CAP	EC15	–	–	–
PE6	–	–	–	SCK1	–	–
PE7	–	–	–	MISO1	–	–
PE8	–	–	–	MOSI1	–	–
PF0(2)(3)	SWDIO	–	–	–	–	–
PF1(2)(3)	SWCLK	–	–	–	–	–
PF2	–	–	–	–	–	–
PF3	SXIN	–	–	–	–	–
PF4	SXOUT	–	–	–	–	–
PF5	XIN	–	–	–	–	–
PF6	XOUT	–	–	–	–	–
PF7	–	–	–	–	–	–
PF8	–	–	–	–	–	–
PF9	–	–	–	–	–	–

NOTES:

1. Unused pins should not be configured as floating inputs.
2. After a reset, the alternate functions of the PF0 and PF1 pins are set as SWDIO and SWCLK, respectively, and the internal pull-down on SWCLK and the internal pull-up on SWDIO are enabled.
3. The SWCLK and SWDIO pins should not be switched to other functions while they are connected to the debugger host.

4. Electrical Characteristics

4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency.

Data based on characterization results, design simulations, and/or technical characteristics are not tested in production but are indicated in the table footnotes.

4.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of T_A = 25°C and VDD = 5.0 V. The typical data are provided only as design recommendations and are not tested.

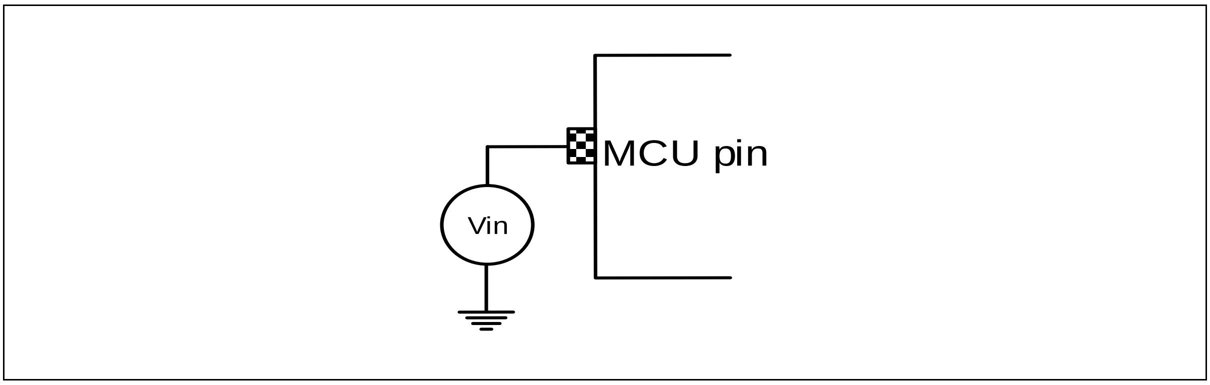
4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

4.1.4 Pin Input Voltage

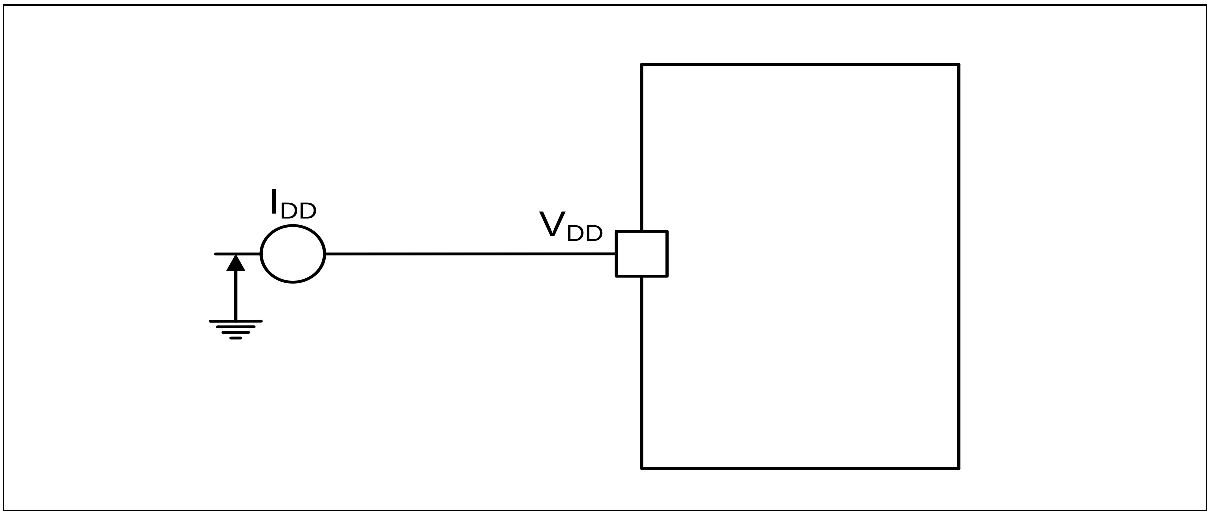
The input voltage measurement on a pin of the device is described in Figure 9.

Figure 9. Pin Input Voltage



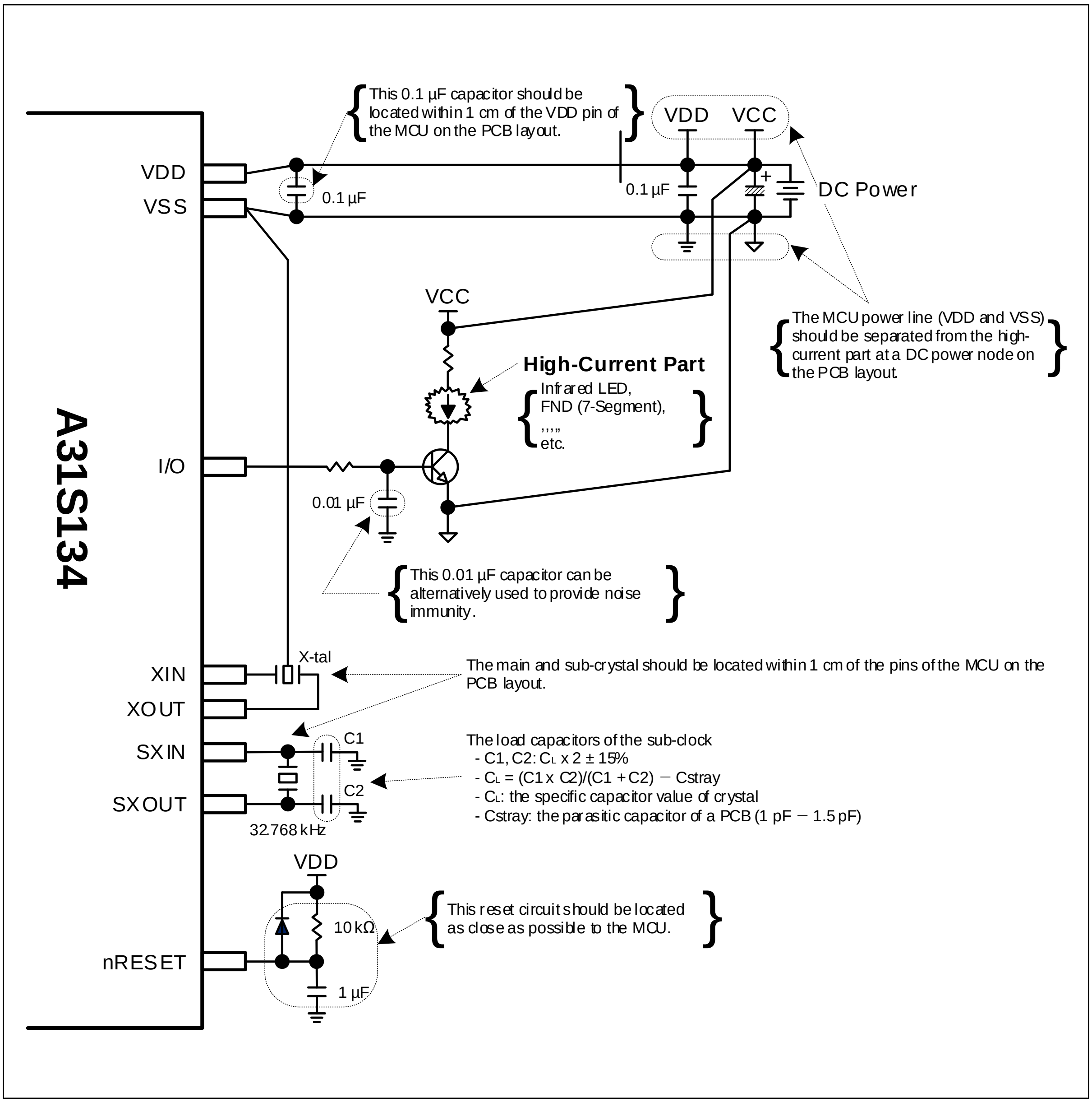
4.1.5 Current Consumption Measurement

Figure 10. Current Consumption Measurement



4.1.6 Power Supply Diagram

Figure 11. Power Supply Diagram



NOTE: Each power supply pair (VDD, VSS, etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

4.2 Absolute Maximum Ratings

Exceeding stresses specified in Table 9 for voltage characteristics, Table 9 for current characteristics, or Table 10 for thermal characteristics may result in permanent damage to the device. The values listed in the tables are stress ratings only and do not imply that the device will function correctly under these conditions. Prolonged exposure to these maximum rating conditions may impact the device's reliability. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

Table 9. Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
$V_{DD} - V_{SS}$(1)	External main supply voltage (including V_{DD})	−0.3	6.5	V
V_I	Input voltage on I/O	−0.3	Max. (V_{DD}) + 0.3	V
V_O	Output voltage on I/O	−0.3	Max. (V_{DD}) + 0.3	V

NOTES:

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.
2. V_I maximum must always be respected.

Table 10. Current Characteristics

Symbol	Description	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD} power lines (source)(1)	170	mA
ΣI_{VSS}	Total current out of sum of all V_{SS} ground lines (sink)(2)	190	mA
I_{OH}	Maximum out current sourced by any I/O and control pin	−18	mA
$\Sigma I_{OH(PIN)}$	Total output current sourced by sum of all I/Os and control pins(2)	−120	mA
$I_{OL1(PIN)}$	Maximum output current sunk by any I/O and control pin	15	mA
$I_{OL2(PIN)}$	Maximum output current sunk by PD[7:0]	120	mA
$\Sigma I_{OL1(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	mA
$\Sigma I_{OL2(PIN)}$	Total output current sunk by sum of all PD[7:0](2)	130	mA
P_T	Total power dissipation	650	mW

NOTES:

1. All main power (V_{DD}) and ground (V_{SS}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.

Table 11. Thermal Characteristics

Symbol	Description	Value	Unit
T_{OP}	Operating temperature (commercial grade)	−40 to 85	°C
	Operating temperature (industrial grade)	−40 to 105	°C
T_{STG}	Storage temperature range	−65 to 150	°C
T_J	Maximum junction temperature	150	°C

4.3 Operating Conditions

4.3.1 Recommended Operating Conditions

Table 12. Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	-	1.8(1)	–	5.5	V
FREQ	Operating frequency	HIRC @ 1.8 ≤ VDD ≤ 5.5	2.0	–	32	MHz
		External clock @ 3.0 ≤ VDD ≤ 5.5	2.0	–	32	MHz
		Main oscillator (ceramic) @ 1.8 ≤ VDD ≤ 5.5	2.0	–	4.2	MHz
		Main oscillator (crystal) @ 2.7 ≤ VDD ≤ 5.5	2.0	–	16	MHz
		Sub-oscillator @ 1.8 ≤ VDD ≤ 5.5	32	–	38	kHz
V_{IN}	I/O input voltage	–	−0.3	–	V_{DD}	V
T_A	Ambient temperature	Commercial @ 1.8 ≤ VDD ≤ 5.5	−40	–	85	°C
		Industrial @ 1.8 ≤ VDD ≤ 5.5	−40	–	105	°C
T_J	Junction temperature	-	−40	–	125	°C

NOTE: When RESET is released, functionality is guaranteed down to V_{LVR} Min.

4.3.2 Power-on Reset Characteristics

Table 13. Power-on Reset Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	–	–	0.1	–	μA
V_{set}	POR setting level	–	–	1.2	–	V
t_R	V_{DD} voltage rising time	0.2 V to 2.0 V	20	–	20,000	μs/V
t_F	V_{DD} voltage falling time	0.2 V to 2.0 V	20	–	20,000	μs/V
V_{reset}	POR reset level	–	–	1.0	–	V
ΔV	Hysteresis voltage	–	–	0.2	–	V

4.3.3 Reset and Power Control Block Characteristics (LVR and LVI)

The parameters listed in Table 14 and Table 15 are obtained through tests conducted under ambient temperature conditions, which are specified in Table 12.

Table 14. Low-Voltage Reset Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{LVR_R}(1)	LVR Rising edge threshold	LVRVS[3:0]	1111	–	1.62	1.77	V
V_{LVR_F}(1)	LVR falling edge threshold	LVRVS[3:0]	1011	1.85	2.00	2.15	
			1010	1.98	2.13	2.28	
			1001	2.13	2.28	2.43	
			1000	2.31	2.46	2.61	
			0111	2.47	2.67	2.87	
			0110	2.84	3.04	3.24	
			0101	3.00	3.20	3.40	
			0100	3.35	3.55	3.75	
			0011	3.45	3.75	4.05	
			0010	3.69	3.99	4.29	
			0001	3.95	4.25	4.55	
			0000	4.25	4.55	4.85	
ΔV	Hysteresis	–		–	100	200	mV
t_{LVRW}	Minimum pulse width	–		100	–	–	μs
–	Noise cancelling time	–		-	2	-	μs
I_{LVR}	LVR current	Enable	V_{DD} = 5 V	–	10.0	20.0	μA
		Disable		–	–	0.1	

NOTE: The LVR threshold is selected by LVRVS[3:0] bits of CONF_LVRCNFIG register in the Configure Option Area.

Table 15. Low-Voltage Indicator Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{LVI_F}(1)(2)	Detection level	Falling edge voltage		1.85	2.00	2.15	V
				1.98	2.13	2.28	
				2.13	2.28	2.43	
				2.31	2.46	2.61	
				2.47	2.67	2.87	
				2.84	3.04	3.24	
				3.00	3.20	3.40	
				3.35	3.55	3.75	
				3.45	3.75	4.05	
				3.69	3.99	4.29	
				3.95	4.25	4.55	
				4.25	4.55	4.85	
ΔV	Hysteresis	–		–	–	200	mV
t_{LVRW}	Minimum pulse width	–		100	–	–	µs
–	Noise cancelling time	–		–	2	–	µs
I_{LVI}	LVI current	Enable, All modes	V_{DD} = 5 V	–	10.0	20.0	µA
		Disable		–	–	0.1	

NOTES:

1. The LVI level can be selected by the SCU_LVICR.LVIVS[3:0] bits.
2. Refer to the low-voltage indicator control register in the user's manual.

4.3.4 Current Consumption Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 16.

4.3.4.1 Supply Voltage and Current Consumption

Table 16. Supply Voltage and Current Characteristics

Symbol	Parameter	Condition		Typ.	Max.	Unit
I_{DD1} (Main RUN)	Supply current	f_{HIRC} = 32 MHz	V_{DD} = 5V ± 10%	5.5	11.0	mA
		f_{HIRC} = 16 MHz	V_{DD} = 5V ± 10%	3.5	7.0	
		f_{XIN} = 16 MHz	V_{DD} = 5V ± 10%	5.0	10.0	
			V_{DD} = 3V ± 10%	3.5	7.0	
I_{DD2} (Main SLEEP)		f_{HIRC} = 32 MHz	V_{DD} = 5V ± 10%	3.4	6.8	mA
		f_{HIRC} = 16 MHz	V_{DD} = 5V ± 10%	2.2	4.4	
		f_{XIN} = 16 MHz	V_{DD} = 5V ± 10%	3.2	6.4	
			V_{DD} = 3V ± 10%	2.0	4.0	
I_{DD3} (Sub-RUN)		f_{SUB} = 32.768 kHz or f_{WDTRC} = 40 kHz V_{DD} = 3V ± 10%, T_A = 25°C		90	180	μA
I_{DD4} (Sub-SLEEP)				7.5	15.0	μA
I_{DD5} (DEEP-SLEEP)		V_{DD} = 5V ± 10%, T_A = 25°C		0.5	3.0	μA

NOTES:

1. Where the f_{XIN} is an external main oscillator, the f_{SUB} is an external sub-oscillator, and the f_{HIRC} is a high frequency internal RC oscillator.
2. All supply current items do not include the current of the WDTRC oscillator and peripheral blocks. However, they include the current of the Power-on Reset (POR) block.

4.3.4.2 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

4.3.4.3 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be simply calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

To estimate the current consumption for output pins, any external pull-down or load must also be taken into consideration.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. Therefore, it is recommended to avoid applying an intermediate voltage level if there is no specific need for this configuration.

4.3.4.4 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

4.3.5 External Clock Source Characteristics

4.3.5.1 External Main Oscillator

The external main oscillator (XMOSC) clock can be generated using a crystal/ceramic resonator oscillator with a frequency range of 2 to 16 MHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 17.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 17. External Main Oscillator Characteristics(1)

Symbol	Parameter	Conditions(2)	Min.	Typ.	Max.	Unit
f_{XMOSC}	XMOSC crystal frequency	V_{DD} = 2.7 V to 5.5 V	2.0	–	16.0	MHz
	XMOSC ceramic oscillator frequency	V_{DD} = 1.8 V to 5.5 V	2.0	–	4.2	
		V_{DD} = 2.7 V to 5.5 V	2.0	–	16.0	
f_{OSC_IN}	XIN input frequency	V_{DD} = 3.0 V to 5.5 V	2.0	–	32.0	MHz
	External clock duty ratio	–	–	50	–	%
R_F	Feedback resistor	XIN = V_{DD}, XOUT = V_{SS}, T_A = 25°C, V_{DD} = 5 V	0.6	1.2	2.0	MΩ
$t_{SU(XMOSC)}$(3)	XMOSC crystal startup time	V_{DD} = 2.7 V to 5.5 V, f_{XMOSC} ≥ 2 MHz	–	–	60	ms
	XMOSC ceramic oscillator startup time	V_{DD} = 1.8 V to 5.5 V, f_{XMOSC} ≥ 2 MHz	–	–	10	
t_{XH}, t_{XL}	Duration of high or low state of XIN input	f_{OSC_IN} = 2.0 to 32 MHz	15.6	–	250	ns

NOTES:

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. $t_{SU(XMOSC)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 2 MHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

Figure 12. Crystal/Ceramic Oscillator

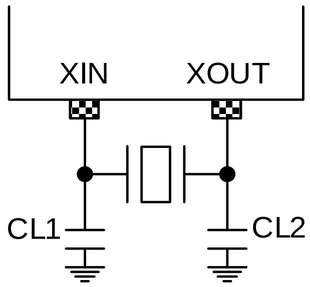


Figure 13. External Clock

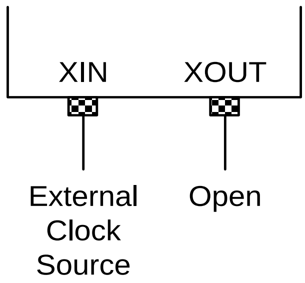
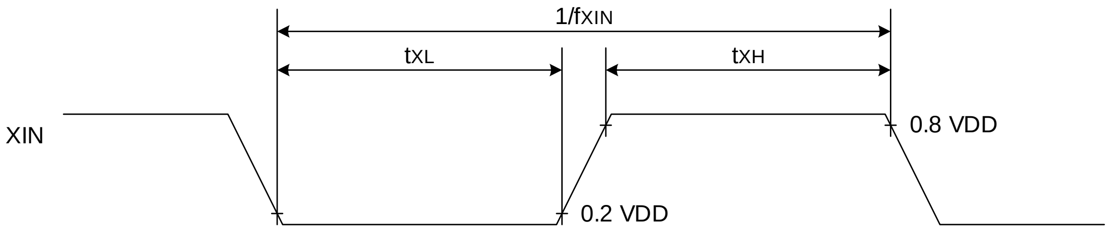


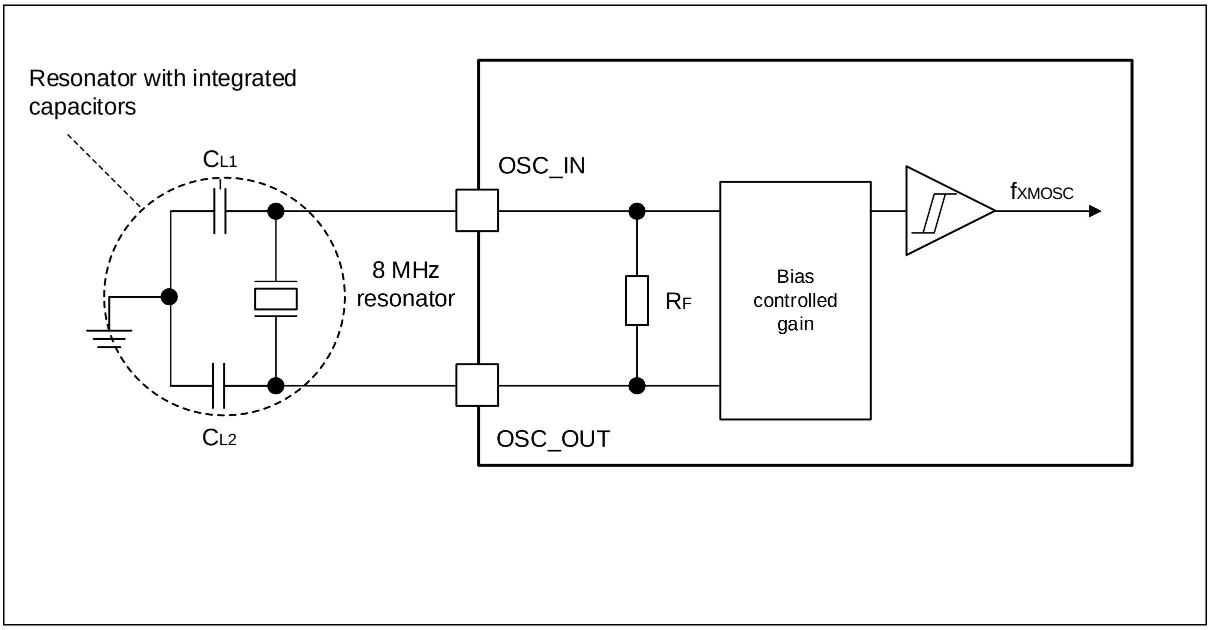
Figure 14. Clock Timing Measurement at XIN



It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The CL1 and CL2 capacitors are usually of the same size, and the crystal manufacturer typically specifies a load capacitance that is the series combination of both capacitors. The capacitance values of the CL1 and CL2 capacitors should be set by considering the parasitic capacitance of the printed circuit board (PCB) and microcontroller pins, which is approximately twice the specified load capacitance of the crystal.

Figure 15 shows a circuit diagram of a typical application with an 8 MHz crystal.

Figure 15. Typical Application with an 8 MHz Crystal



4.3.5.2 External Sub-oscillator

The external sub-oscillator (XSOSC) clock can be generated using a crystal/ceramic resonator oscillator with a frequency of 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 18.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

Table 18. External Sub-oscillator Characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{XSOSC}	XSOSC oscillator frequency	1.8 V to 5.5 V	32	32.768	38	kHz
f_{OSC_SXIN}	SXIN input frequency	1.8 V to 5.5 V	32	–	38	kHz
R_F	Feedback resistor	SXIN = V_{DD}, SXOUT = V_{SS}, T_A = 25°C, V_{DD} = 5 V	2.5	5.0	10.0	MΩ
$t_{SU(XSOSC)}$(2)	XSOSC crystal startup time	–	–	–	10	s
		V_{DD} = 3 V, T_A = 25°C		0.7	1.5	
$t_{XH / XL}$	Duration of high or low state of SXIN input	–	13	–	15	μs

NOTES:

1. Guaranteed by design.
2. $t_{SU(XSOSC)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator, and it can vary significantly with the crystal manufacturer.

Figure 16. Crystal Oscillator

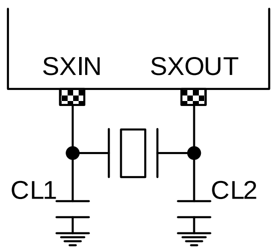


Figure 17. External Clock

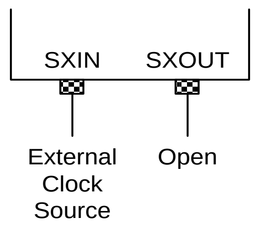


Figure 18. Clock Timing Measurement at SXIN

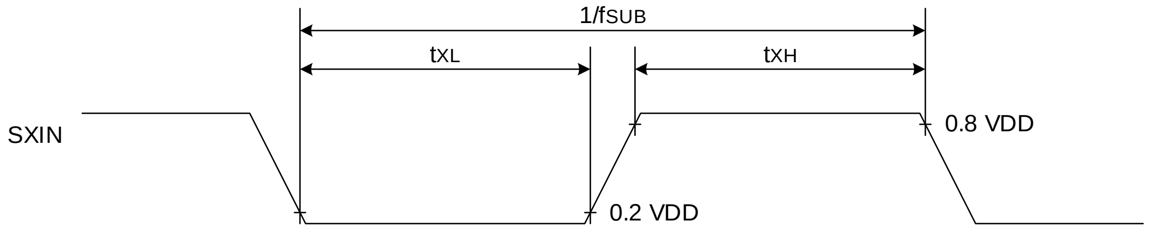
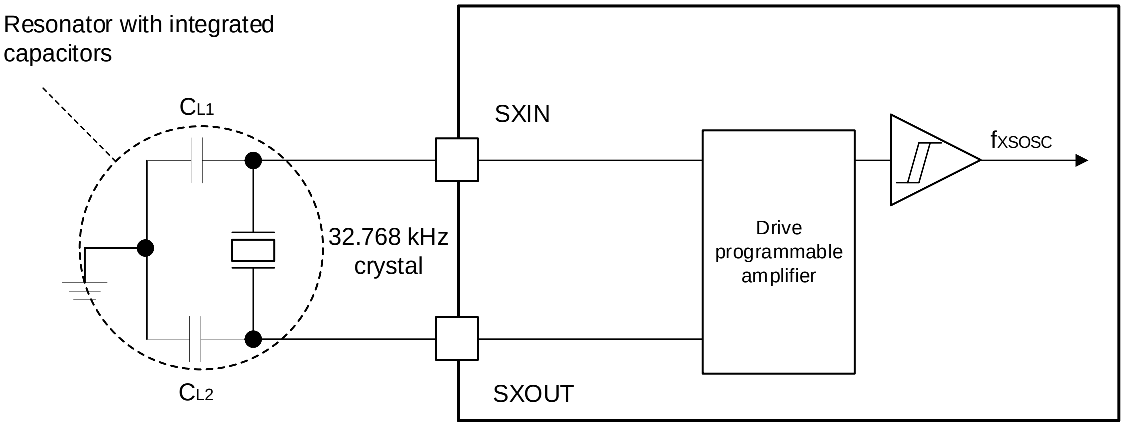


Figure 19. Typical Application with a 32.768 kHz Crystal



NOTE: An external resistor is not required between SXIN and SXOUT and it is forbidden to add one.

4.3.6 Internal Clock Source Characteristics

The parameters listed in Table 19 and Table 20 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 12.

4.3.6.1 High-Speed Internal RC Oscillator

Table 19. High-Speed Internal RC Oscillator Characteristics

Symbol	Parameter	Conditions(2)	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	–	1.8	–	5.5	V
f_{HIRC}	HIRC frequency	–	–	32	–	MHz
ACC_{HIRC}(1)	Accuracy	T_A = 0°C to 50°C	–	–	±1.5	%
		T_A = −10°C to 50°C Exclusively utilizing E-PGM+ for User Trimming(2)	–	–	±1.0	
		T_A = –40°C to 85°C (commercial)	–	–	±2.0	
		T_A = –40°C to 105°C (industrial)	–	–	±3.0	
DuCy	Duty cycle	–	40	50	60	%
$t_{STAB(HIRC)}$	HIRC oscillator stabilization time	–	–	–	100	µs
I_{HIRC}	HIRC oscillator power consumption	HIRC oscillator is enabled.	–	500	–	µA
		HIRC oscillator is disabled.	–	–	0.1	

NOTES:

1. Guaranteed by design, but it may require on-board programming after the SMT process. Calibration of the HIRC at high temperatures can result in frequency shifts, so it is important to ensure sufficient calibration time for cooling to near room temperature after the SMT process.
2. User Trimming refers to the calibration process of adjusting the frequency of the HIRC oscillator using E-PGM+. It is a method used to fine-tune the accuracy of the oscillator. To achieve a tolerance of ±1.0% for the HIRC frequency, it is necessary to perform User Trimming.

4.3.6.2 Internal WatchDog Timer RC Oscillator

Table 20. Internal WatchDog Timer RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{WDTRC}	WDTRC frequency	–	34	40	46	kHz
$t_{STAB(WDTRC)}$	WDTRC stabilization time	–	–	–	1	ms
I_{WDTRC}	WDTRC power consumption	WDTRC is enabled.	–	3	6	µA
		WDTRC is disabled.	–	–	0.1	

4.3.7 Flash Memory Characteristics

Table 21. Flash Memory Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
t_{FSW}	Page write time	–		–	3.0	3.5	ms
t_{FSE}	Page erase time	–		–	3.0	3.5	ms
t_{FCE}	Chip erase time	–		–	3.0	3.5	ms
V_{PGM}	Programming voltage	During erase / write		2.0	–	5.5	V
f_{HCLK}	System clock frequency	–		2.0	–	–	MHz
NF_{FWE}	Endurance of code flash memory (write / erase operation)	Page 0 to 511 Configuration option page 1	T_A = 25°C Page unit	10,000	–	–	cycles
		Configuration option page 2/3		100,000	–	–	
NF_{DFWE}	Endurance of data flash memory (write / erase operation)	Page 0 to 127	T_A = 25°C Page unit	100,000	–	–	cycles
t_{FRT}	Retention time	–		10	–	–	years

4.3.8 I/O Port Characteristics

The parameters listed in Table 22 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 12.

Table 22. DC Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	All input ports, nRESET		$0.8 \times V_{DD}$	–	V_{DD}	V
V_{IL}	Input low voltage	All input ports, nRESET		–	–	$0.2 \times V_{DD}$	V
V_{OH1}	Output high voltage	V_{DD} = 4.5 V, I_{OH1} = −2 mA, All output ports except V_{OH2}		V_{DD} – 1.0	–	–	V
V_{OH2}		V_{DD} = 4.5 V, T_A = 25°C, I_{OH2} = −15 mA, PE[8:0], PC5		V_{DD} – 2.0	–	–	
V_{OL1}	Output low voltage	V_{DD} = 4.5 V, I_{OL1} = 10 mA, All output ports except V_{OL2}		–	–	1.0	V
V_{OL2}		V_{DD} = 4.5 V, I_{OL2} = 120 mA, PD[7:0]		–	1.5	3.0	
I_{IH}	Input high leakage current	All input ports		–	–	1	μA
I_{IL}	Input low leakage current	All input ports		–1	–	–	μA
R_{PU}	Pull-up resistor	V_I = 0 V, T_A = 25°C All input ports	V_{DD} = 5 V	25	50	100	kΩ
			V_{DD} = 3 V	50	100	200	
		V_I = 0 V, T_A = 25°C nRESET	V_{DD} = 5 V	150	250	400	
			V_{DD} = 3 V	300	500	700	
R_{PD}	Pull-down resistor	V_I = V_{DD}, T_A = 25°C All input ports	V_{DD} = 5 V	13	25	50	kΩ
			V_{DD} = 3 V	25	50	100	
C_{IO}	I/O pin capacitance	F = 1 MHz Unmeasured pins are connected to V_{SS}.		–	–	10	pF

4.3.8.1 Output Driving Current

The GPIOs are capable of sinking or sourcing currents within the range specified by I_{OL} and I_{OH}.

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on V_{DD} and the maximum operating current of the microcontroller on V_{DD} (during Run mode) must not exceed the absolute maximum rating ΣI_{VDD} specified in Table 10.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during Run mode) must not exceed the absolute maximum rating ΣI_{VSS} specified in Table 10.

4.3.8.2 Output Voltage Characteristics

Unless otherwise specified, the parameters in Table 23 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 12.

Table 23. Output Voltage Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OH1}	Output high level voltage for an I/O pin	V_{DD} = 4.5V, I_{OH1} = –2 mA	V_{DD} – 1.0	–	–	V
V_{OH2}		V_{DD} = 4.5V, I_{OH2} = –15 mA	V_{DD} – 2.0	–	–	V
V_{OL1}	Output low level voltage for an I/O pin	V_{DD} = 4.5V, I_{OL1} = 10 mA	–	–	1.0	V
V_{OL2}		V_{DD} = 4.5V, I_{OL2} = 120 mA	–	1.5	3.0	V

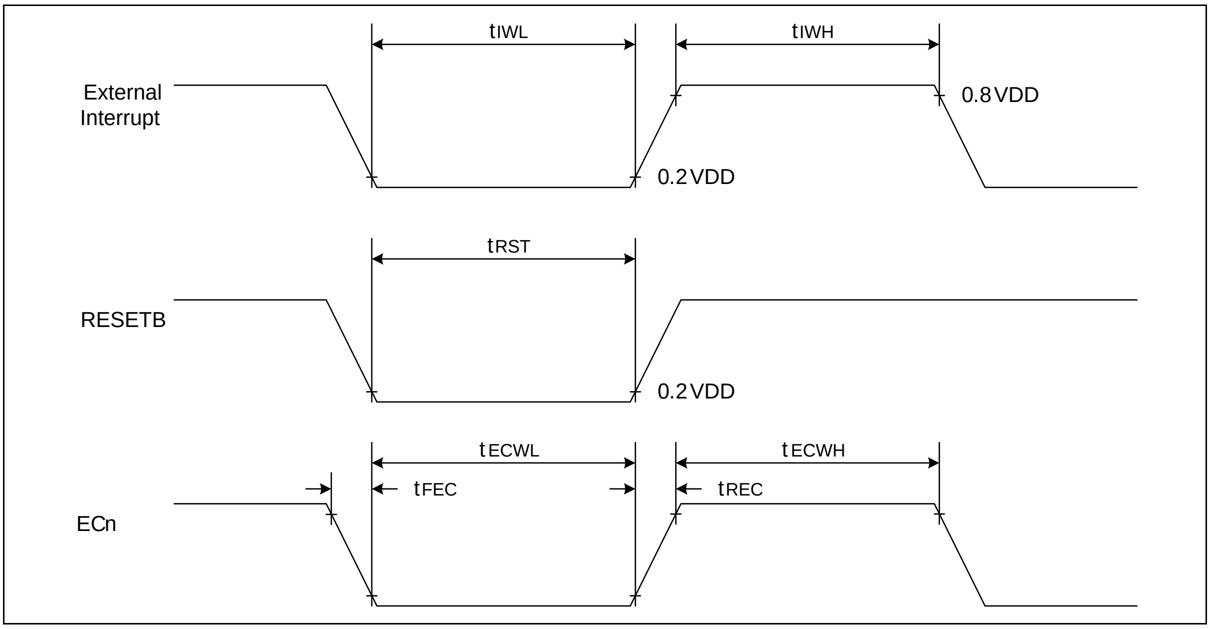
4.3.8.3 AC Characteristics

Unless otherwise specified, the parameters in Table 24 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 12.

Table 24. AC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{RST}	RESETB input low width	V_{DD} = 5 V	10	–	–	μs
t_{IWH}, t_{IWL}	Interrupt input high, low width	V_{DD} = 5 V, all interrupts	100	–	–	ns
t_{ECWH}, t_{ECWL}	External counter input high, low pulse width	V_{DD} = 5 V, all external counter inputs	100	–	–	ns
t_{REC}, t_{FEC}	External counter transition time	V_{DD} = 5 V, all external counter inputs	–	–	20	ns
f_{IO}	I/O frequency	V_{DD} = 2.7 V, C_L = 30 pF	–	–	8	MHz

Figure 20. AC Timing



4.3.9 Analog-to-Digital Converter Characteristics

Unless otherwise specified, the parameters in Table 25 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 12.

Table 25. ADC Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	–		2.2	-	5.5	V
–	Resolution	–		–	12	–	bit
V_{AN}	Analog input voltage	–		V_{SS}	–	AV_{REF}	V
AV_{REF}	Analog reference voltage	–		2.2	–	V_{DD}	V
I_{ADC}	ADC current	ADC is enabled.	V_{DD} = 5.0 V	–	1	2	mA
		ADC is disabled.		–	–	0.1	μA
I_{AN}	ADC input leakage current	AV_{REF} = 5.0 V		–	–	2	μA
t_{CONV}	Conversion time	2.7 V ≤ AV_{REF} ≤ 5.5 V		20	–	–	μs
PCLK	Operating frequency	–		2	–	32	MHz
INL	Integral non-linearity	2.7 V ≤ AV_{REF} ≤ 5.5 V		–	–	±5	LSB
DNL	Differential non-linearity	2.7 V ≤ AV_{REF} ≤ 5.5 V		–	–	±1	
ZOE(1)	Zero-offset error	2.7 V ≤ AV_{REF} ≤ 5.5 V		–	–	±4	
FSE(2)	Full-scale error	2.7 V ≤ AV_{REF} ≤ 5.5 V		–	–	±8	
		V_{DD} = 3 V, when VDD is used as the ADC reference voltage		–	–	+30	

NOTES:

1. The zero offset error is the discrepancy between the value of 0x000 and the converted output value when a zero-input voltage (V_{SS}) is applied.
2. The full-scale error is the discrepancy between the value of 0xFFF and the converted output value when the full-scale voltage (V_{DD}) is applied.
3. When AV_{REF} is below 2.7 V, the resolution degrades by 1 bit for every 0.1 V drop in AV_{REF}. The resolution has not been tested below 2.7 V. It is recommended to use a 0.5 MHz ADC clock when operating the ADC below 2.7 V.

4.3.9.1 General PCB Design Guidelines

The power supply must be separated in accordance with the scheme shown in Figure 11. The de-coupling capacitors across the V_{DD}/AV_{DD} are ceramic (good quality) capacitors and must be placed as close as possible to the chip.

4.3.10 Communication Interface Characteristics

4.3.10.1 I2C Interface Characteristics

The I2C interface conforms to the timing requirements specified in the I2C-bus specification, in addition to the user timing requirements listed below:

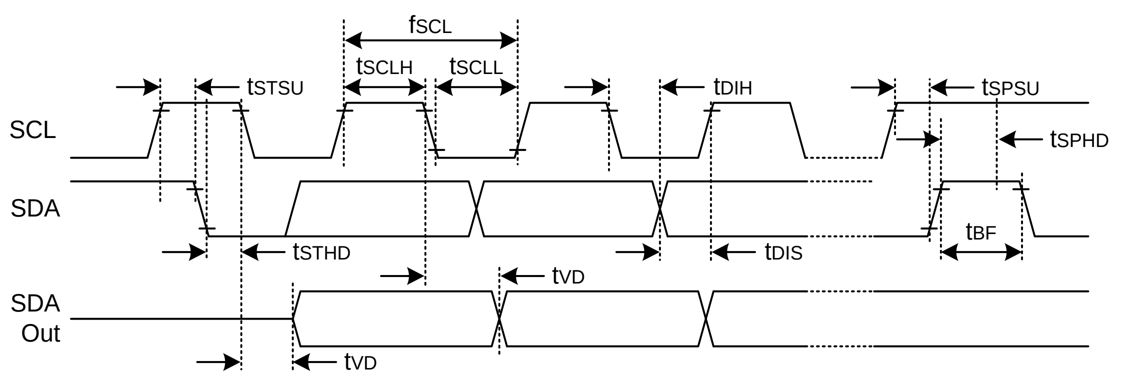
- Standard mode (Sm): up to 100 kbps bit rate
- Fast mode (Fm): up to 400 kbps bit rate
- Fast mode plus (Fm+): up to 1 Mbps bit rate

The I2C timing requirements are guaranteed by design when the I2C peripheral is configured correctly and the I2C clock frequency is equal to or greater than the minimum value listed in the table below.

Table 26. I2C Characteristics

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
–	I2C Operating voltage	$V_{DD} \geq 1.8$ V		$V_{DD} \geq 2.0$ V		$V_{DD} \geq 2.7$ V		V
f_{SCL}	Clock frequency	0	100	0	400	0	1,000	kHz
t_{SCLH}	Clock high pulse width	4.0	–	0.6	–	0.26	–	μs
t_{SCLL}	Clock low pulse width	4.7	–	1.3	–	0.5	–	μs
t_{BF}	Bus free time	4.7	–	1.3	–	0.5	–	μs
t_{STSU}	Start condition setup time	4.7	–	0.6	–	0.26	–	μs
t_{STHD}	Start condition hold time	4.0	–	0.6	–	0.26	–	μs
t_{SPSU}	Stop condition setup time	4.0	–	0.6	–	0.26	–	μs
t_{SPHD}	Stop condition hold time	4.0	–	0.6	–	0.26	–	μs
t_{VD}	Output valid from clock	0	–	0	–	0	–	μs
t_{DIH}	Data input hold time	0	–	0	1.0	0	0.45	μs
t_{DIS}	Data input setup time	250	–	100	–	50	–	ns

Figure 21. I2C Timing



4.3.10.2 SPI Interface Characteristics

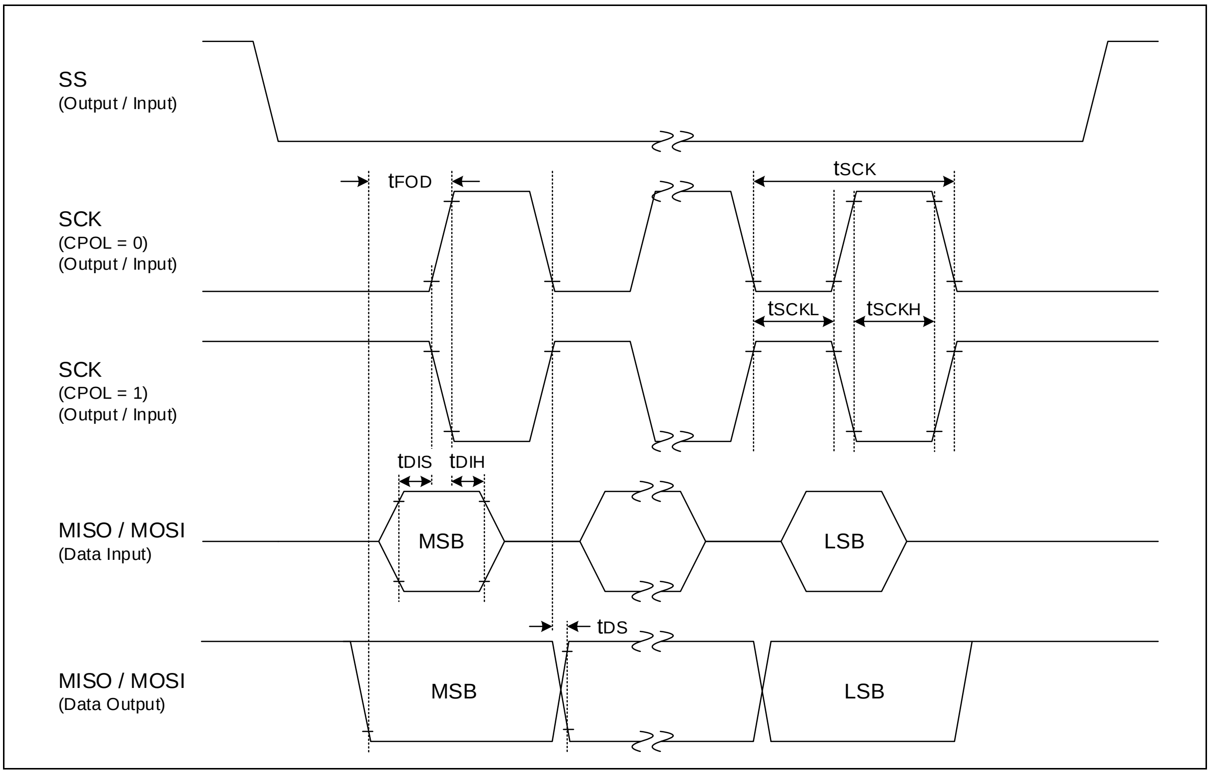
Unless otherwise specified, the parameters in Table 27 are obtained through tests conducted under ambient temperature, f_{PCLK} frequency and supply voltage conditions, which are specified in Table 12.

For more information about I/O alternate function characteristics (SS, SCK, MOSI, and MISO for SPI), refer to 4.3.8.

Table 27. SPI Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
f_{SCK}	SPI clock frequency	VDD ≥ 2.7 V	Internal SCK source	–	–	8	MHz
			External SCK source				
		VDD ≥ 1.8 V	Internal SCK source	–	–	4	
			External SCK source				
t_{SCKH}, t_{SCKL}	Input / output clock high, low pulse width	Internal / External SCK source		0.8 × Typ.	$t_{SCK}/2$	1.2 × Typ.	ns
t_{FOD}	First output clock delay time	Internal / External SCK source, CPHA = 0		0.4 x t_{SCK}	–	–	ns
t_{DS}	Output clock delay time	–		–	–	25	ns
t_{DIS}	Input setup time			17	–	–	ns
t_{DIH}	Input hold time			20	–	–	ns
Duty	Duty cycle of SPI frequency (SCK)	Slave mode		40	50	60	%

Figure 22. SPI Timing



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4.3.10.3 UART Interface Characteristics

Unless otherwise specified, the parameters in Table 28 are obtained through tests conducted under ambient temperature, f_{PCLK} frequency and supply voltage conditions, which are specified in Table 12.

Table 28. UART Characteristics

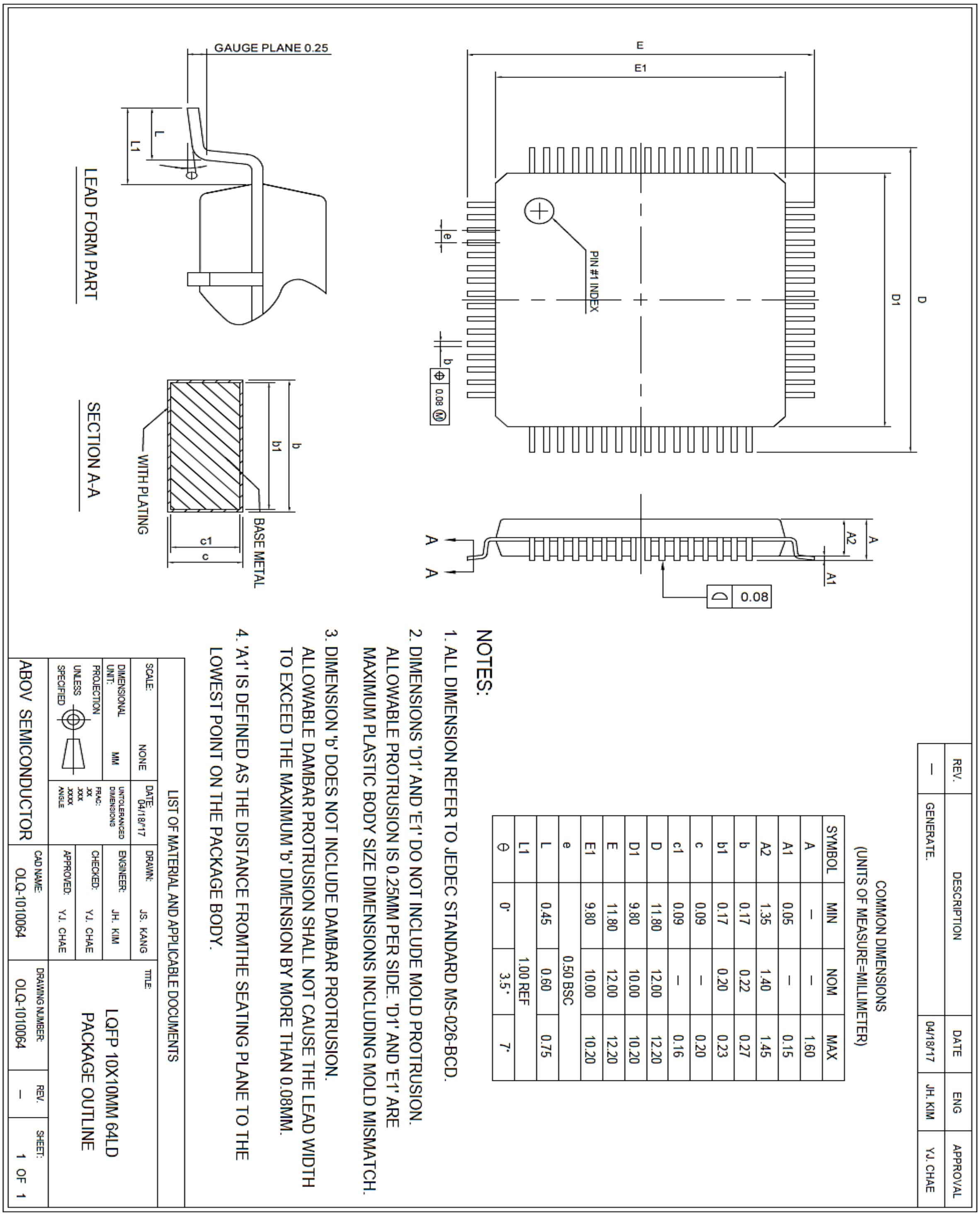
Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{max}	Maximum character transmission frequency	–	–	0.32	Mbps

5. Package Information

5.1 64-LQFP Package Information

64-LQFP is a 64-pin, 10 x 10 mm Quad Flat Package.

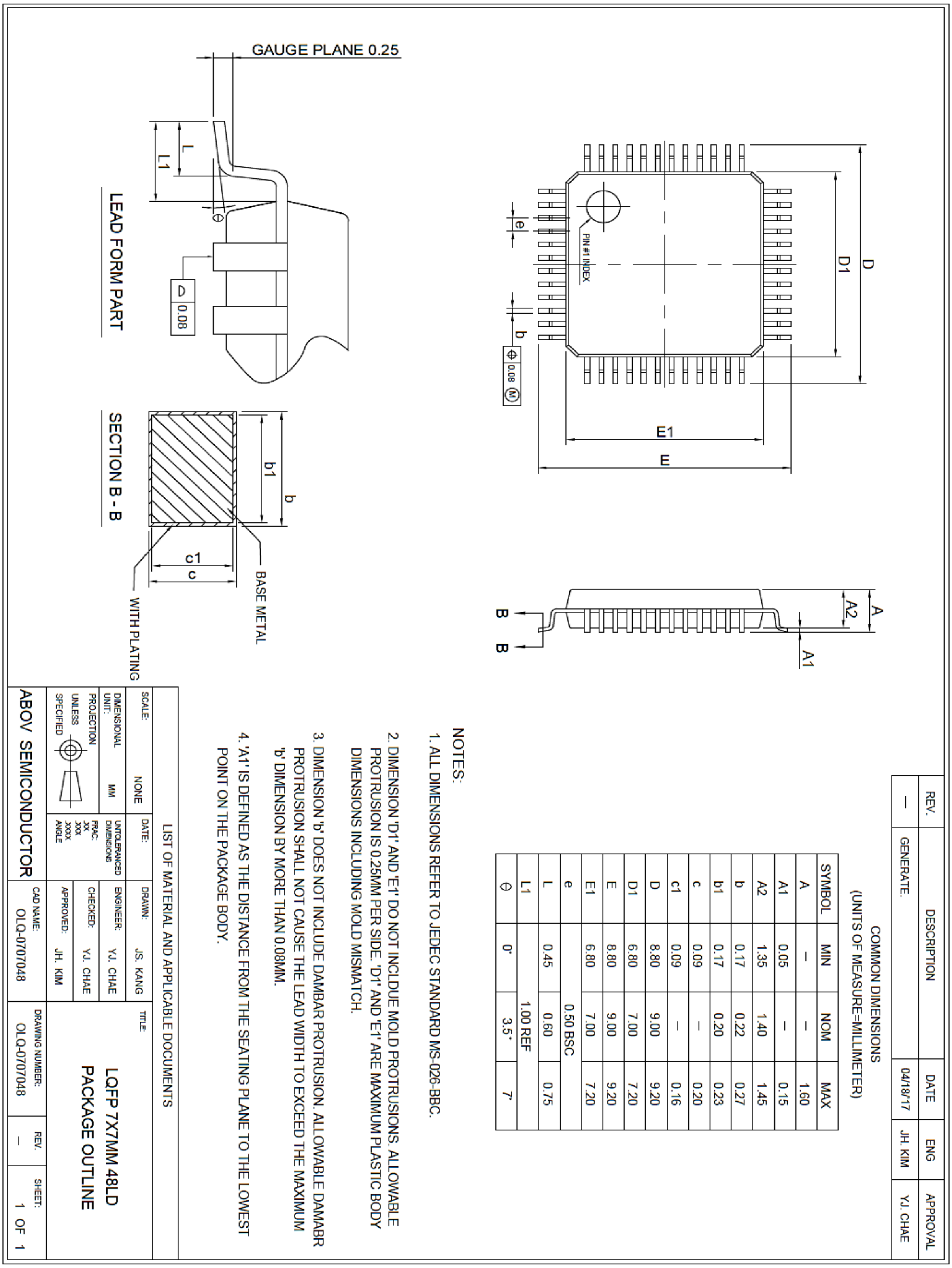
Figure 23. 64-LQFP Package Dimension



5.2 48-LQFP Package Information

48-LQFP is a 48-pin, 7 x 7 mm Quad Flat Package.

Figure 24. 48-LQFP Package Dimension

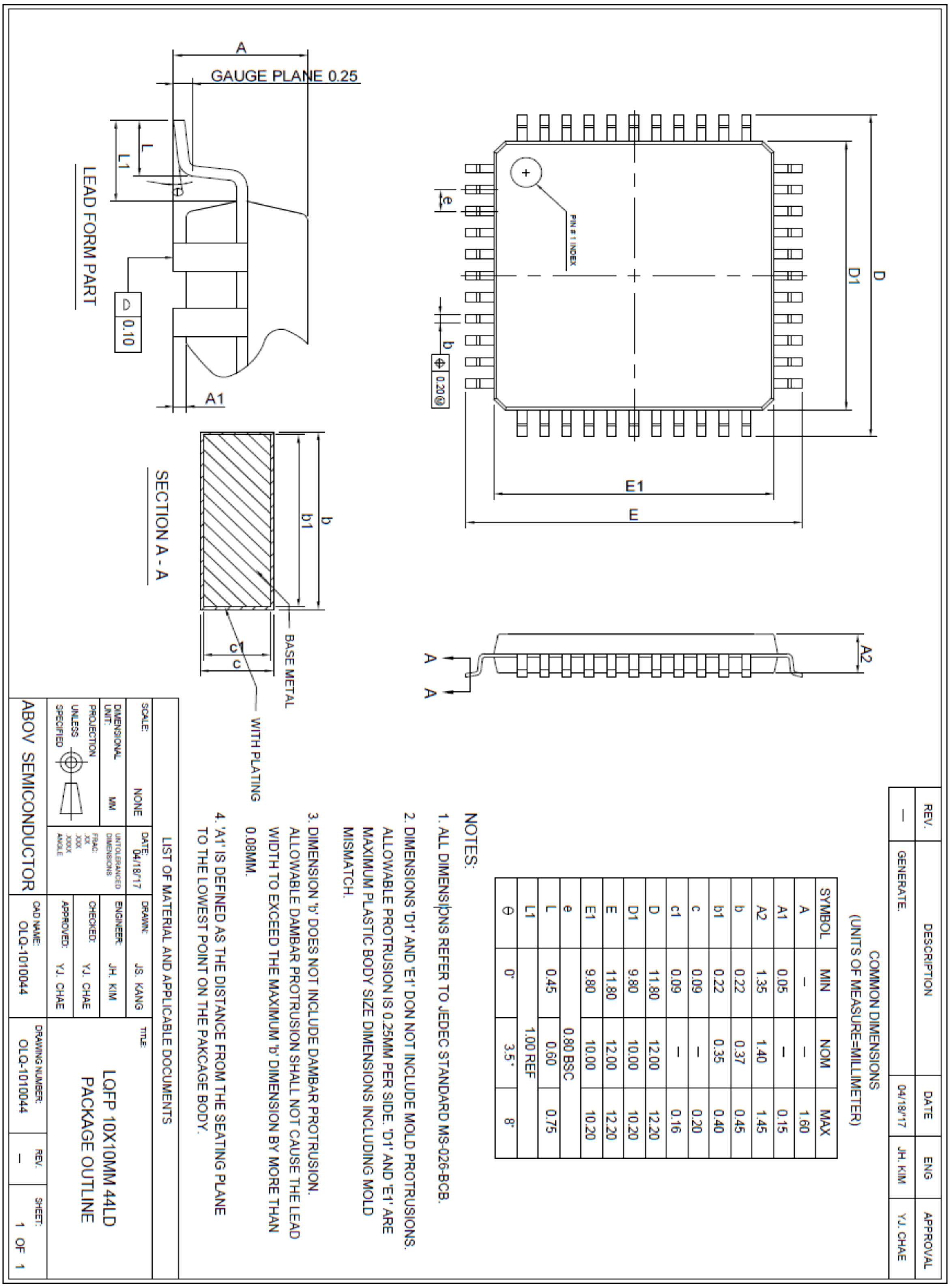


SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

5.3 44-LQFP Package Information

44-LQFP is a 44-pin, 10 x 10 mm Quad Flat Package.

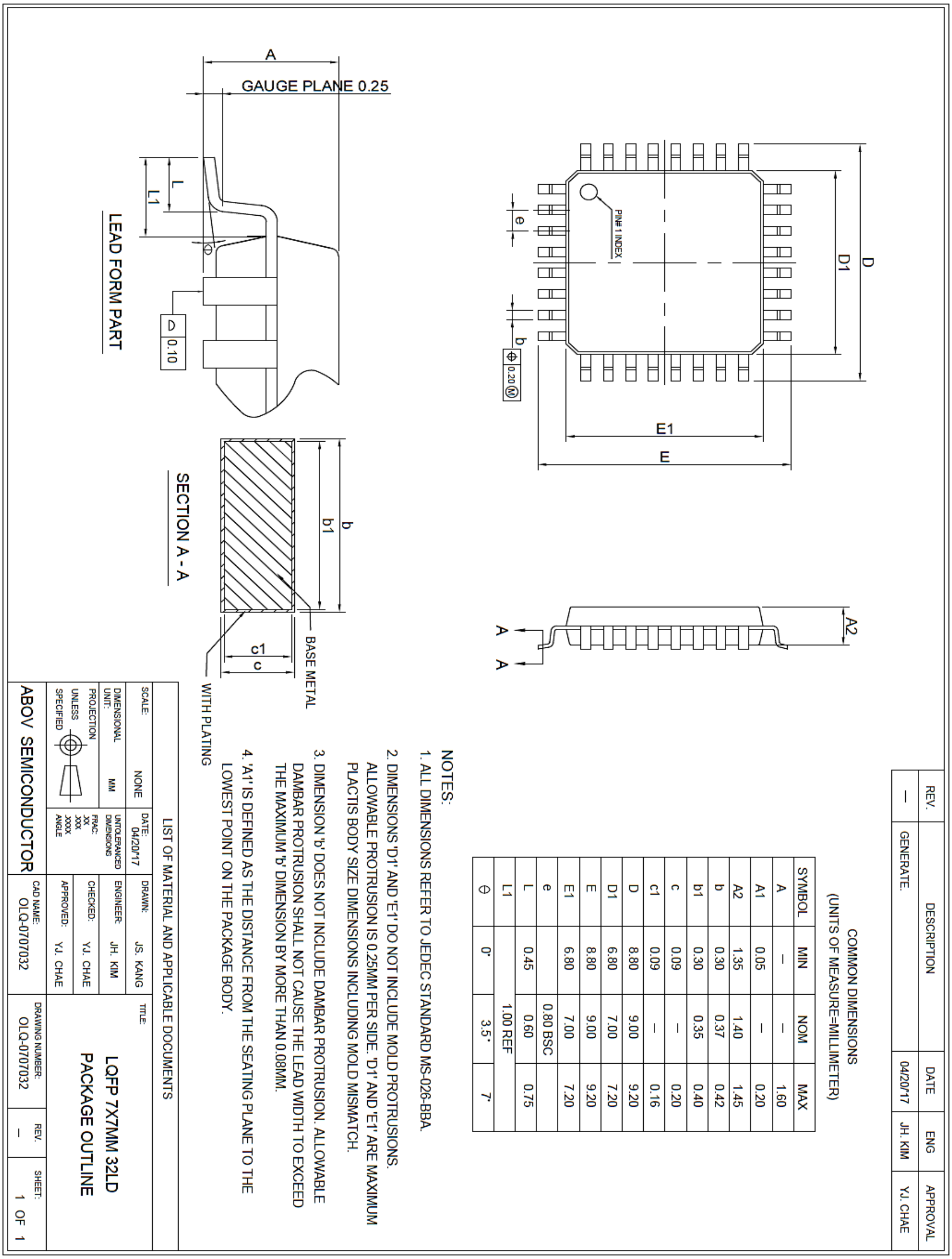
Figure 25. 44-LQFP Package Dimension



5.4 32-LQFP Package Information

32-LQFP is a 32-pin, 7 x 7 mm Quad Flat Package.

Figure 26. 32-LQFP Package Dimension



SYMBOL	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
b	0.30	0.37	0.42
b1	0.30	0.35	0.40
c	0.09	—	0.20
c1	0.09	—	0.16
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.80 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°	3.5°	7°

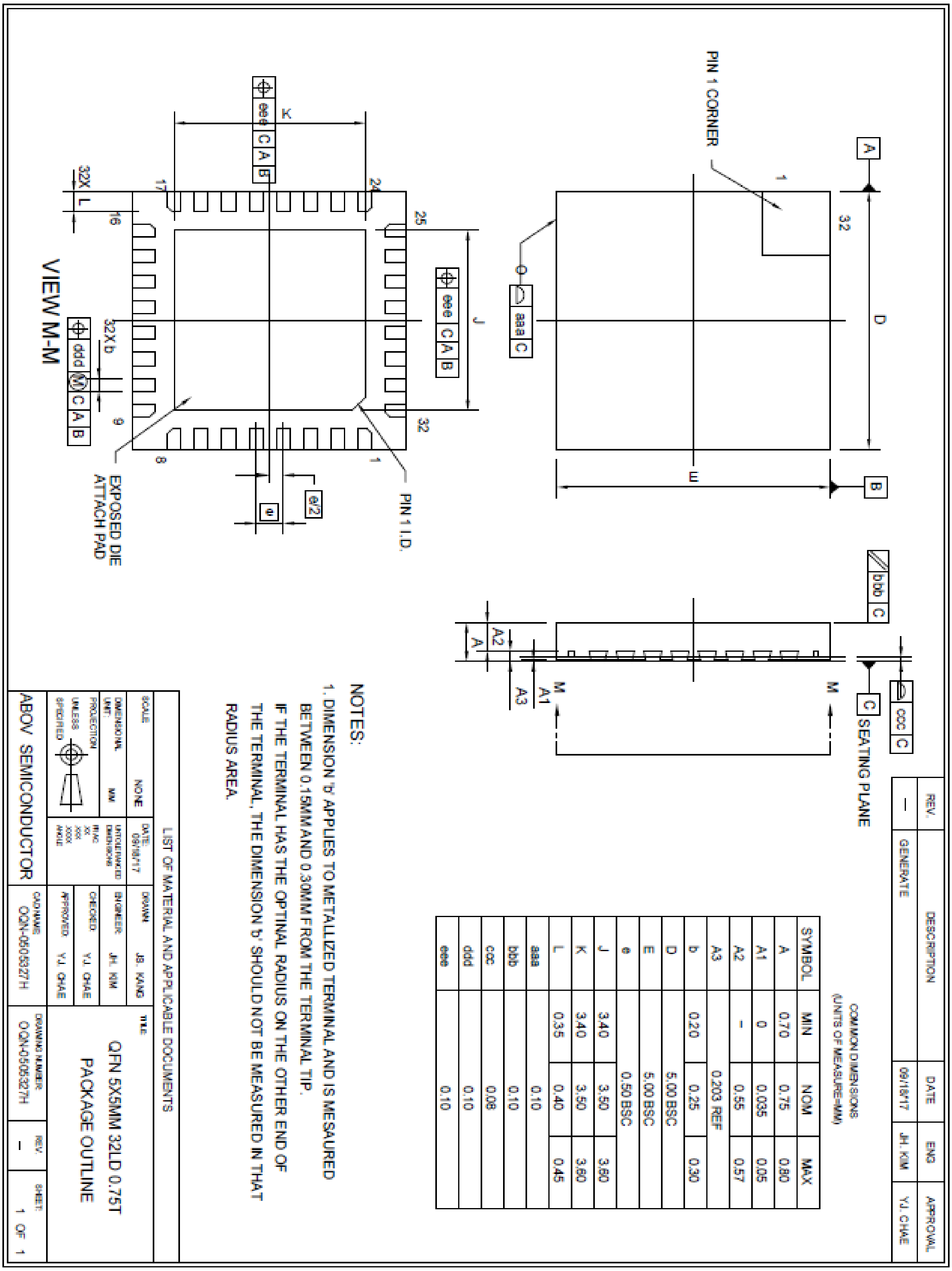
NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026-BBA.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. 'D1' AND 'E1' ARE MAXIMUM PLACTIS BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM 'b' DIMENSION BY MORE THAN 0.08MM.
4. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

5.5 32-QFN Package Information

32-QFN is a 32-pin, 5 x 5 mm Quad Flat No-lead package.

Figure 27. 32-QFN Package Dimension



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.035	0.05
A2	-	0.55	0.57
A3		0.203 REF	
b	0.20	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
J	3.40	3.50	3.60
K	3.40	3.50	3.60
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

6. Ordering Information

Figure 28. Device Nomenclature - Part Number Decoder

A31S13 4 R L 2 N (T)

Device family name

A31S13 = Arm Cortex-M0+ based microcontroller

Code memory size

4	128 Kbytes

Pin count

R	64-pin
C	48-pin
S	44-pin
K	32-pin

Package type

L	LQFP1 (0.5 mm pin pitch)
N	LQFP3 (0.8 mm pin pitch)
U	QFN

Temperature

None	−40 to 85°C (commercial grade)
2	−40 to 105°C (industrial grade)

Bonding wire

None	Au wire
N	Pd-Cu wire

Packing

(T)	Tape & reel
(W)	Wafer
(C)	Chip carrier

NOTE: For a list of available options (memory, package, and so on) or for further information on any aspect of this device, contact the nearest ABOV sales office.

Glossary

This section gives a brief definition of acronyms, abbreviations and terminology used in this document:

- AHB: Advanced High-performance Bus
- APB: Advanced Peripheral Bus
- Byte: Data of 8-bit length
- CRC: Cyclic Redundancy Check
- DMA: Direct Memory Access
- I2C: Inter-Integrated Circuit
- LSB: Least Significant Bit
- LQFP: Low-profile Quad Flat Package
- LVI: Low-Voltage Indicator
- LVR: Low-Voltage Reset
- PGM: Programming
- POR: Power-On Reset
- QFN: Quad Flat No-Lead
- SCU: System Control Unit
- SPI: Serial Peripheral Interface
- UART: Universal Asynchronous Receiver Transmitter
- USART: Universal Synchronous and Asynchronous Receiver Transmitter
- WDT: WatchDog Timer
- Word: Data of 32-bit length

Revision History

Revision	Date	Notes
1.00	Aug 18, 2023	Initial release
1.01	Dec 29, 2023	Minor revision
1.02	July 5, 2023	Minor revision
1.03	July 8, 2024	Minor revision
1.04	Dec 2, 2024	Updated the disclaimer.

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