# A96L116 Datasheet

# Ultra-Low Power 8-bit Microcontroller, Flash Memory 16 KB, SRAM 1 KB, 12-bit ADC, RTCC and 128-bit Unique ID

DS Rev. 1.03

## Features

### Core

- M8051 8-bit core (8051 Compatible, 2 clocks per cycle)

### Memory

- 16 Kbytes On-Chip Flash Memory
- 256 bytes IRAM, 768 bytes XRAM
- 256 bytes Data Flash Memory

### General-Purpose I/O (GPIO)

- Normal I/O: 18 ports

### Timer/Counter

- Basic Interval Timer (BIT) 8-bit × 1-ch
- WatchDog Timer (WDT) 8-bit × 1-ch
- 16-bit × 3-ch (T0/T1/T2)

### Programmable Pulse Generation

- Pulse Generation (T0/T1/T2)

### Real-Time Clock/Calendar (RTCC)

- Hour, Day, Week, Month, Year

### 12-bit A/D Converter

- Eight Input channels
- Conversion time: 9 us at 2.7 V

### Communication Interface

- 8-bit I2C × 1-ch
- 8-bit SPI × 1-ch
- Low-Power UART
  - — Up to 9,600 bps with 32.768 kHz

### 128-Bit Unique ID

### 16-bit CRC/Checksum Generator

### Power-On Reset

- Reset release level (1.2 V)

### Low-Voltage Reset

- 8-detection level (1.5 V to 2.78 V)

### Low-Voltage Indicator

- 7-detection level (1.87 V to 2.78 V)

### Interrupt Sources

- Seven external Interrupt sources
- 11 internal interrupt sources

### Internal High Frequency RC Oscillator

- 16 MHz ±1.5% ($T_A$ = 0°C to +50°C)
  ±2.0% ($T_A$ = –40°C to +85°C)

### Internal Low Frequency RC Oscillator

- 40 kHz ±15% ($T_A$= –40°C to +85°C)

### Power-down Mode

- STOP, IDLE mode

### Operating Voltage and Frequency

- 1.71 V to 3.6 V @ 32 to 38 kHz with SX-tal
- 1.8 V to 3.6 V @ 0.4 to 4.2 MHz with Ceramic
- 2.0 V to 3.6 V @ 0.4 to 4.2 MHz with X-tal
- 2.7 V to 3.6 V @ 0.4 to 12 MHz with X-tal
- 1.71 V to 3.6 V @ 0.5 to 16 MHz with HFIRC
- 1.71 V to 3.6 V @ 40 kHz with LFIRC

### Operating Temperature

- –40°C to +85°C

### Package Type

- 10-SSOP, 16-SOPN, 20-TSSOP, 20-QFN
- Pb-free

# Product Selection Table

**Table 1. Device Summary**

| Part Number | Flash | IRAM/ XRAM | Data Flash | LPUART | I2C | SPI | Timer | ADC | I/O | Package |
|---|---|---|---|---|---|---|---|---|---|---|
| A96L116FR | 16 KB | 256/768 B | 256 B | 1 | 1 | 1 | 3 | 8-ch | 18 | 20-TSSOP |
| A96L116FU | 16 KB | 256/768 B | 256 B | 1 | 1 | 1 | 3 | 8-ch | 18 | 20-QFN-0404 |
| A96L116AE | 16 KB | 256/768 B | 256 B | 1 | 1 | 1 | 3 | 7-ch | 14 | 16-SOPN |
| A96L116DS | 16 KB | 256/768 B | 256 B | 1 | 1 | 0 | 3 | 4-ch | 8 | 10-SSOP |

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# 1. Introduction

This document provides an overview of the features supported by the device, including high-level information and brief explanations for each feature. Refer to Table 3 for the list of features supported by the device.

# 2. Description

A96L116 is an advanced CMOS Ultra-Low Power 8-bit microcontroller. It has 16 Kbytes of flash memory, 256 bytes data flash memory, 256 bytes of IRAM, 768 bytes of XRAM, General-Purpose I/O, basic interval timer, watchdog timer, 16-bit timer/counter, 16-bit PPG output, real time clock/calendar, LPUART, SPI, I2C, 12-bit A/D converter, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. A96L116 supports power-down modes reducing power consumption.

## 2.1 Product Category Definition

Table 2 provides an overview of the memory capacity for the A96L116.

**Table 2. A96L116 Memory Capacity**

| Memory Capacity | | | | Category |
|---|---|---|---|---|
| **Code Flash** | **IRAM** | **XRAM** | **Data Flash** | |
| 16 KB | 256 B | 768 B | 256 B | A96L116 |

## 2.2 Device Overview

Table 3. A96L116 Features summarizes and lists the features specific to the device while considering the largest package and Table 4. Summary of A96L116 Peripherals shows the features and the number of peripherals in the A96L116 products.

**Table 3. A96L116 Features**

| Item | | Description |
|---|---|---|
| CPU | | • 8-bit CISC core (M8051, 2 clocks per cycle) |
| Memory | Code Flash | • 16 Kbytes with self-read/write capability<br>• On-chip debug and ISP<br>• Endurance: 10,000 cycles |
| | Data Flash | • 256 bytes<br>• Endurance: 100,000 cycles |
| | IRAM | • 256 bytes |
| | XRAM | • 768 bytes |
| GPIO | | • Normal I/O<br>• 18 ports: P0[7:0], P1[5:0], P2[3:0] |
| Timer/Counter | | • BIT 8-bit × 1-ch<br>• WDT 8-bit × 1-ch: 5 kHz internal RC oscillator for WDT<br>• 16-bit × 3-ch (T0/T1/T2)<br>• Real time clock/calendar (RTCC) |
| Programmable Pulse Generation | | • Pulse generation (T0/T1/T2) |
| ADC | | • 12-bit ADC, 8 input channels |
| CRC and Checksum Generator | | • CRC-16 polynomial: 0x8C81 ($X^{16} + X^{15} + X^{11} + X^{10} + X^{7} + 1$)<br>• Auto and user CRC/checksum mode |
| Reset | Power-On Reset | • Reset release level (1.2 V) |
| | Low-Voltage Reset | • 8-detection level (1.5 V to 2.78 V) |
| Low-Voltage Indicator | | • 7-detection level (1.87 V to 2.78 V) |
| Seral Interface | | • Low power UART, up to 9,600 bps with 32.768kHz<br>• I2C × 1, SPI × 1 |
| High-Frequency Internal RC Oscillator | | • 16 MHz ±2.0% ($T_A$ = –40°C to +85°C) |
| Low-Frequency Internal RC Oscillator | | • 40 kHz ±15% ($T_A$ = –40°C to +85°C) |

**Table 3. A96L116 Features (continued)**

| Item | Description |
|---|---|
| Power Consumption | • 94 µA/MHz in Run mode,<br>• 12 µA in Run mode (32.768 kHz, 40 kHz)<br>• 0.35 µA in Stop mode without RTCC<br>• 0.9 µA in Stop mode with RTCC and 32.768 kHz<br>• 5 µs wakeup time from idle/stop modes |
| Operating Voltage and Frequency | • 1.71 V to 3.6 V @ 32 to 38 kHz with SX-tal<br>• 1.8 V to 3.6 V @ 0.4 to 4.2 MHz with Ceramic<br>• 2.0 V to 3.6 V @ 0.4 to 4.2 MHz with X-tal<br>• 2.7 V to 3.6 V @ 0.4 to 12 MHz with X-tal<br>• 1.71 V to 3.6 V @ 0.5 to 16 MHz with HFIRC<br>• 1.71 V to 3.6 V @ 40 kHz with LFIRC |
| Minimum Instruction Execution Time | • 0.125 µs @ 16 MHz IRC |
| Operating Temperature | • –40°C to +85°C |
| Package Type | • Four types of package options (Pb-free)<br>- 20-TSSOP (0.65 mm pitch)<br>- 20-QFN (0.5 mm pitch)<br>- 16-SOPN (1.27 mm pitch)<br>- 10-SSOP (1.0 mm pitch) |

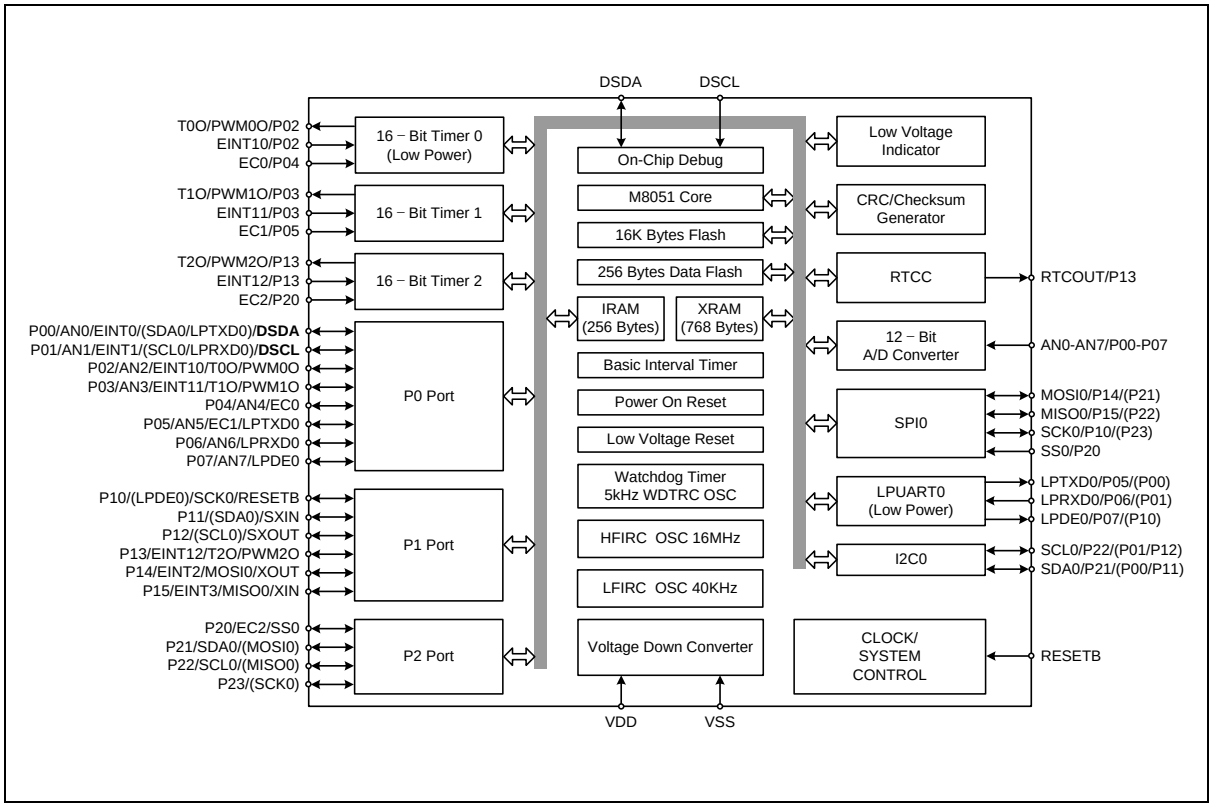
**Table 4. Summary of A96L116 Peripherals**

| Peripheral | | A96L116FR | A96L116FU | A96L116AE | A96L116DS |
|---|---|---|---|---|---|
| Code Flash Memory | | 16 KB | 16 KB | 16 KB | 16 KB |
| Data Flash Memory | | 256 B | 256 B | 256 B | 256 B |
| IRAM/XRAM | | 256 / 768 B | 256 / 768 B | 256 / 768 B | 256 / 768 B |
| Timers | General-Purpose | 3 (16-bit) | | | |
| | WDT | 1 | | | |
| | BIT | 1 | | | |
| Communication Interfaces | SPI | 1 | 1 | 1 | 0 |
| | I2C | 1 | 1 | 1 | 1 |
| | LPUART | 1 | 1 | 1 | 1 |
| RTCC | | 1 | | | |
| GPIO | | 18 | 18 | 14 | 8 |
| ADCs | | 111.1 ksps | 111.1 ksps | 111.1 ksps | 111.1 ksps |
| Number of Channels | | 8 | 8 | 7 | 4 |
| Max. CPU Frequency | | 16 MHz | | | |
| 128 Unique ID | | 1 | | | |
| CRC/Checksum | | 1 (16-bit) | | | |
| Operating Voltage | | 1.71 V to 3.6 V | | | |
| Operating Temperature | | Ambient operating temperature: –40°C to +85°C | | | |
| Packages | | 20-TSSOP | 20-QFN | 16-SOPN | 10-SSOP |

## 2.3 Block Diagram

Figure 1 shows a block diagram of the A96L116.

**Figure 1. A96L116 Block Diagram**



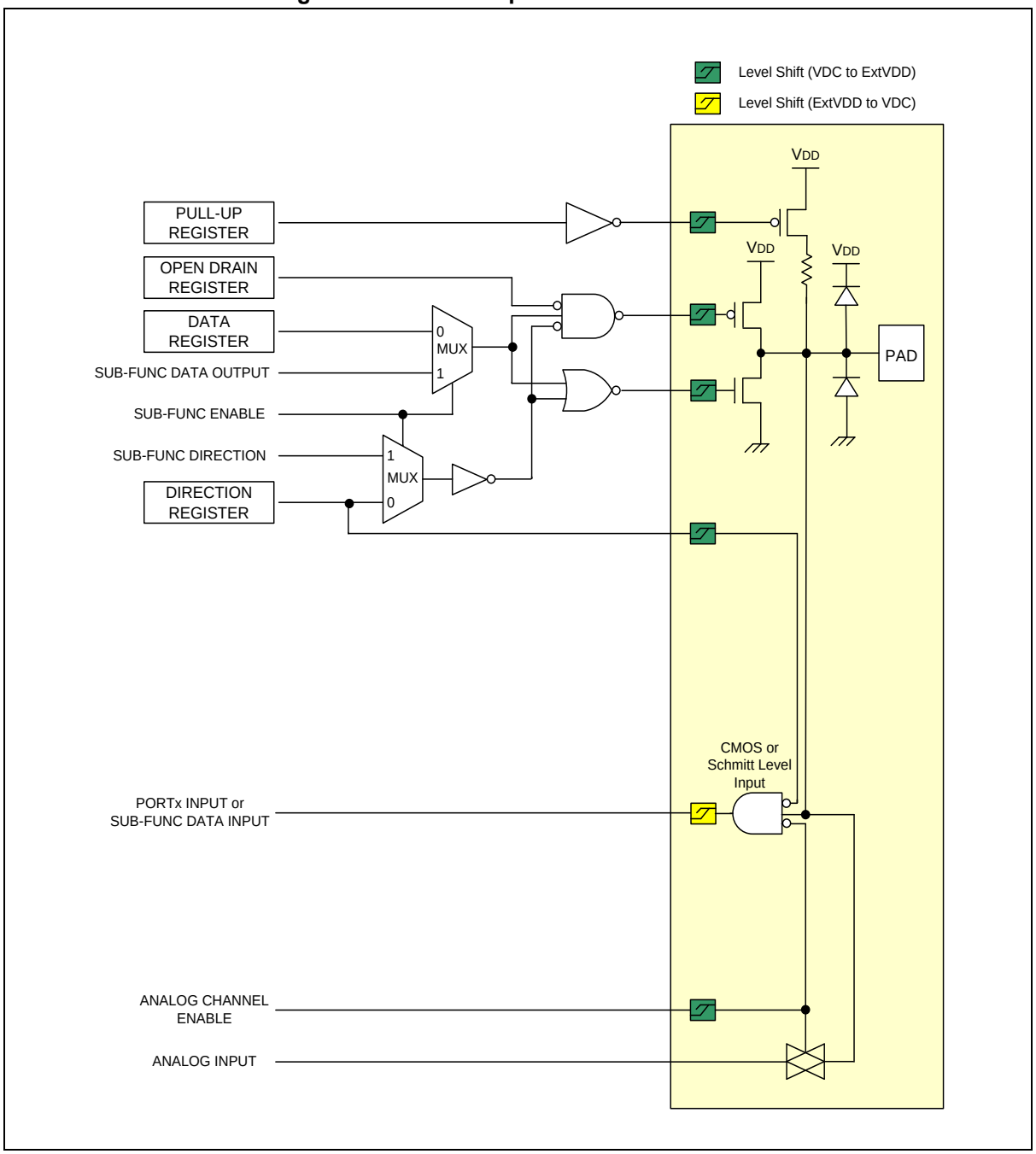
## 2.4 Functional Overview

The following sections provide overviews of the features of the A96L116 microcontroller.

### 2.4.1 Port Structures

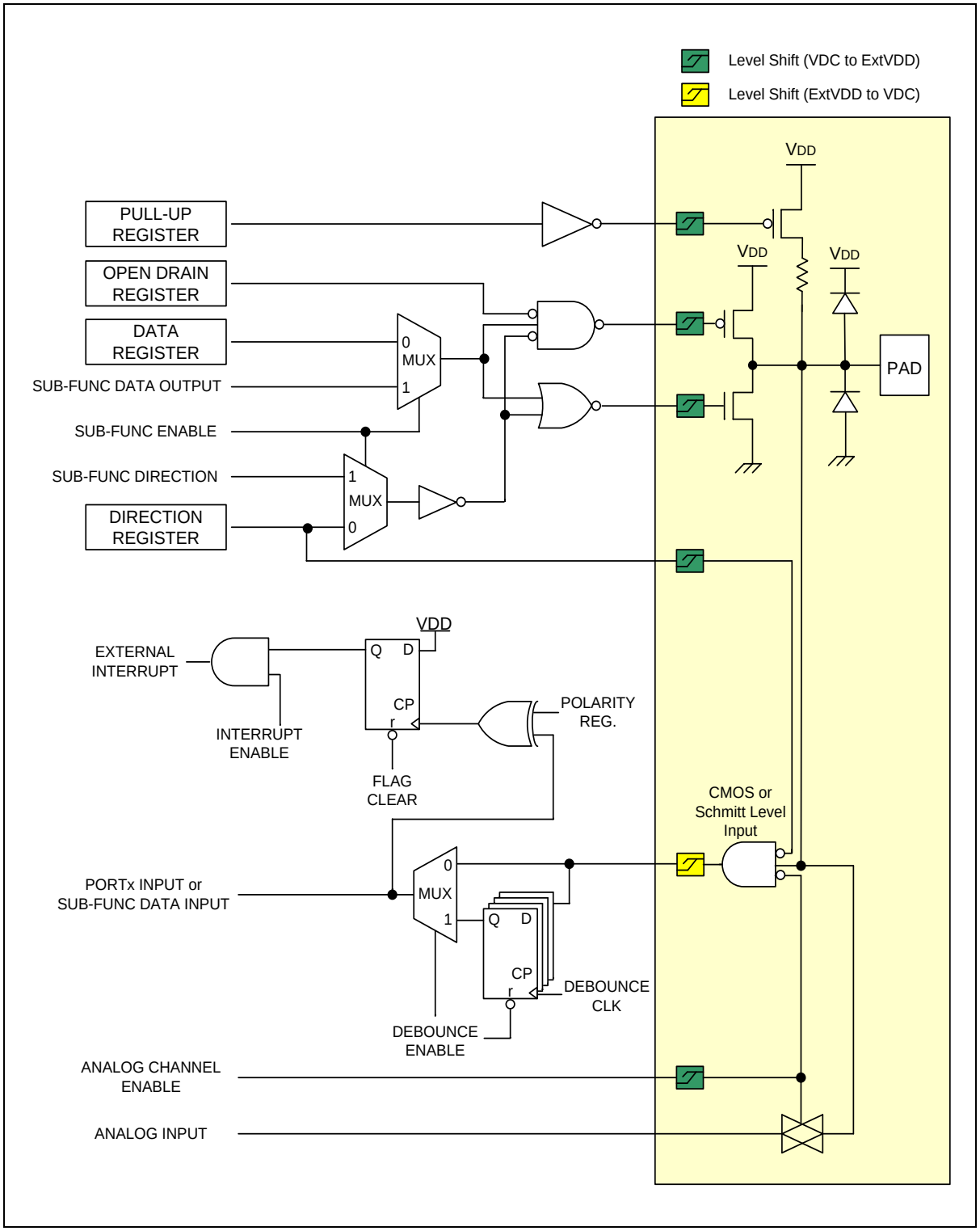
#### 2.4.1.1 GPIO Port Structure

**Figure 2. General-Purpose I/O Port Structure**



### 2.4.1.2 External Interrupt I/O Port Structure

**Figure 3. External Interrupt I/O Port Structure**



### 2.4.2 Memory Organization

A96L116 addresses three separate memory spaces:

- Program memory
- Data memory
- XRAM memory

By means of this logical separation of the memory, 8-bit CPU address can access the data memory more rapidly. 16-bit data memory address is generated through the DPTR register.

A96L116 provides on-chip 16 Kbytes of ISP type flash program memory, which is readable and writable. Internal data memory (IRAM) is 256 bytes, and it includes the stack area. External data memory (XRAM) is 768 bytes.

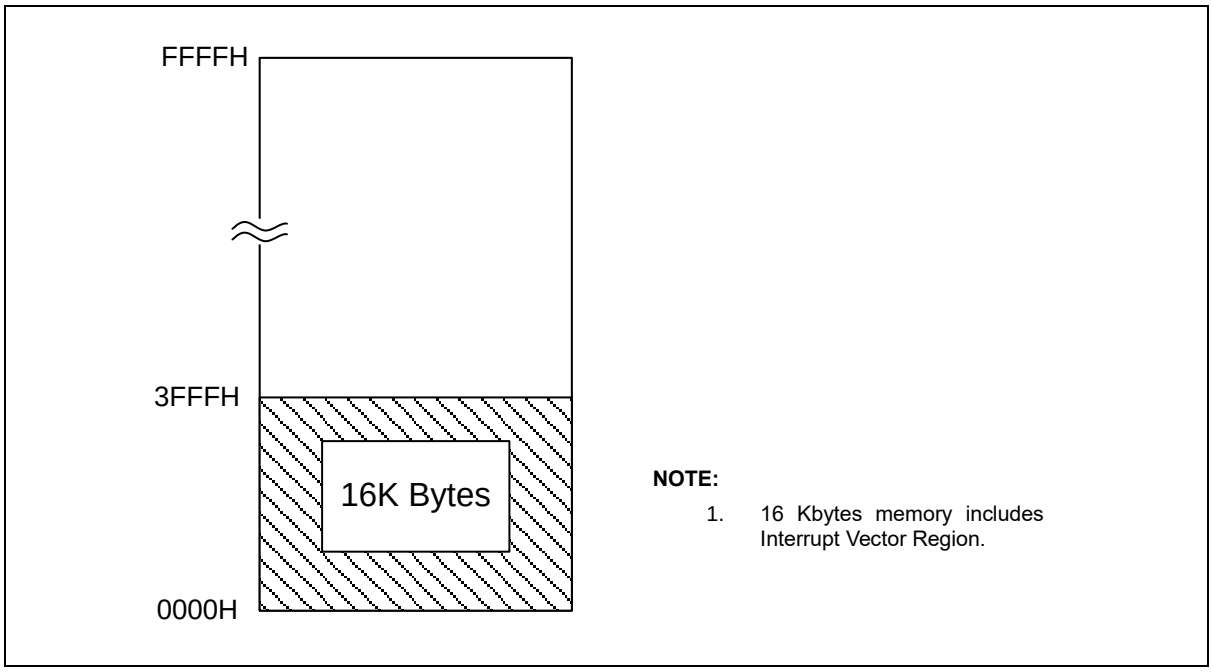
#### 2.4.2.1 Program Memory

A 16-bit Program Counter can address up to 64 Kbytes, but A96L116 has only 16 Kbytes program memory space. After reset, CPU begins execution from location 0000H. Each interrupt is assigned to a fixed location of the program memory. The interrupt causes the CPU to jump to that location, where it commences an execution of a service routine.

For example, an external interrupt 1 is assigned to location 002BH. If the external interrupt 1 is going to be used, its service routine must begin at location 002BH. If the interrupt is not going to be used, its service location is available as general-purpose program memory. If an interrupt service routine is short enough (frequent cases with a control application), the service routine can reside entirely within an 8 bytes interval.

A longer service routine can use a jump instruction to skip over subsequent interrupt locations if other interrupts are in use. Figure 4 shows a map of the lower part of the program memory.

**Figure 4. Program Memory**




More detailed description of program memory is described in chapter 2.4.18 Flash .

#### 2.4.2.2 Internal Data Memory

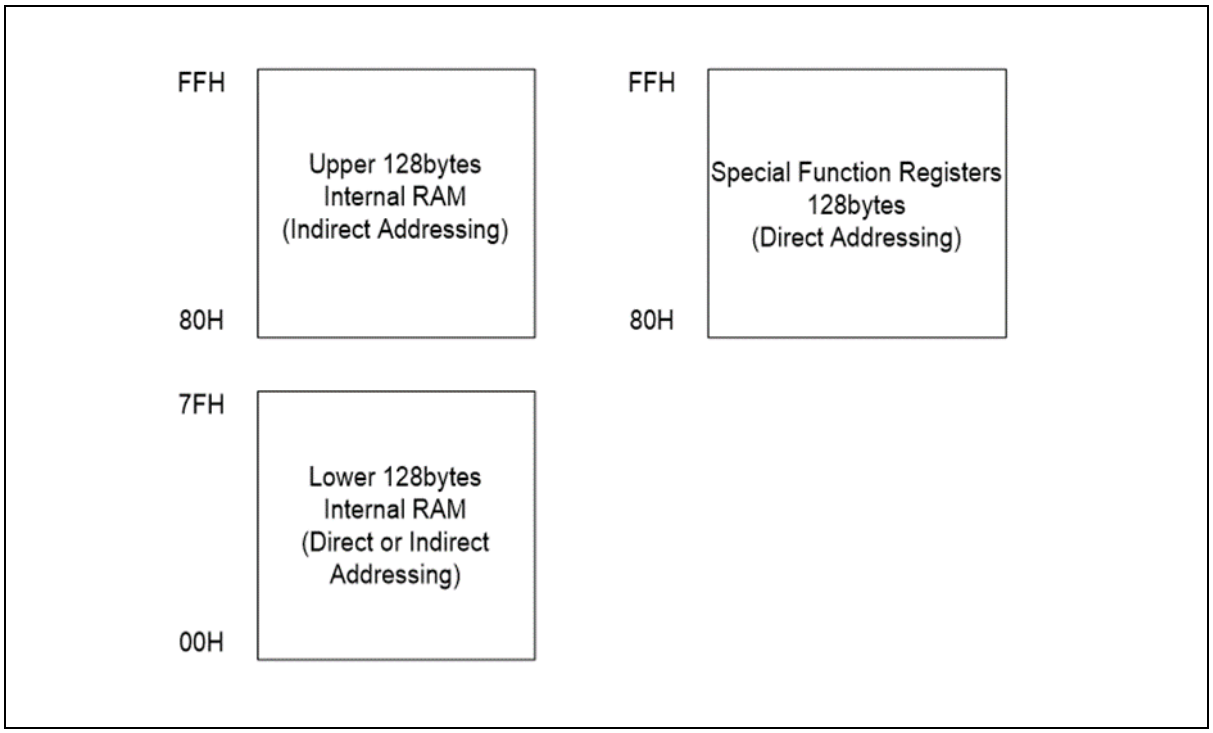
Internal data memory is divided into three spaces as shown in Figure 5. Those three spaces are generally called as,

- Lower 128 bytes
- Upper 128 bytes
- Special Function Registers (SFR space)

Internal data memory addresses are always one byte wide, which implies an address space of 256 bytes.

In fact, the addressing modes of the internal data memory can accommodate up to 384 bytes by using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. By means of this method, the upper 128 bytes and SFR space can occupy the same block of addresses, 80H through FFH, although they are physically separate entities as shown in Figure 5.

**Figure 5. Internal Data Memory Map**

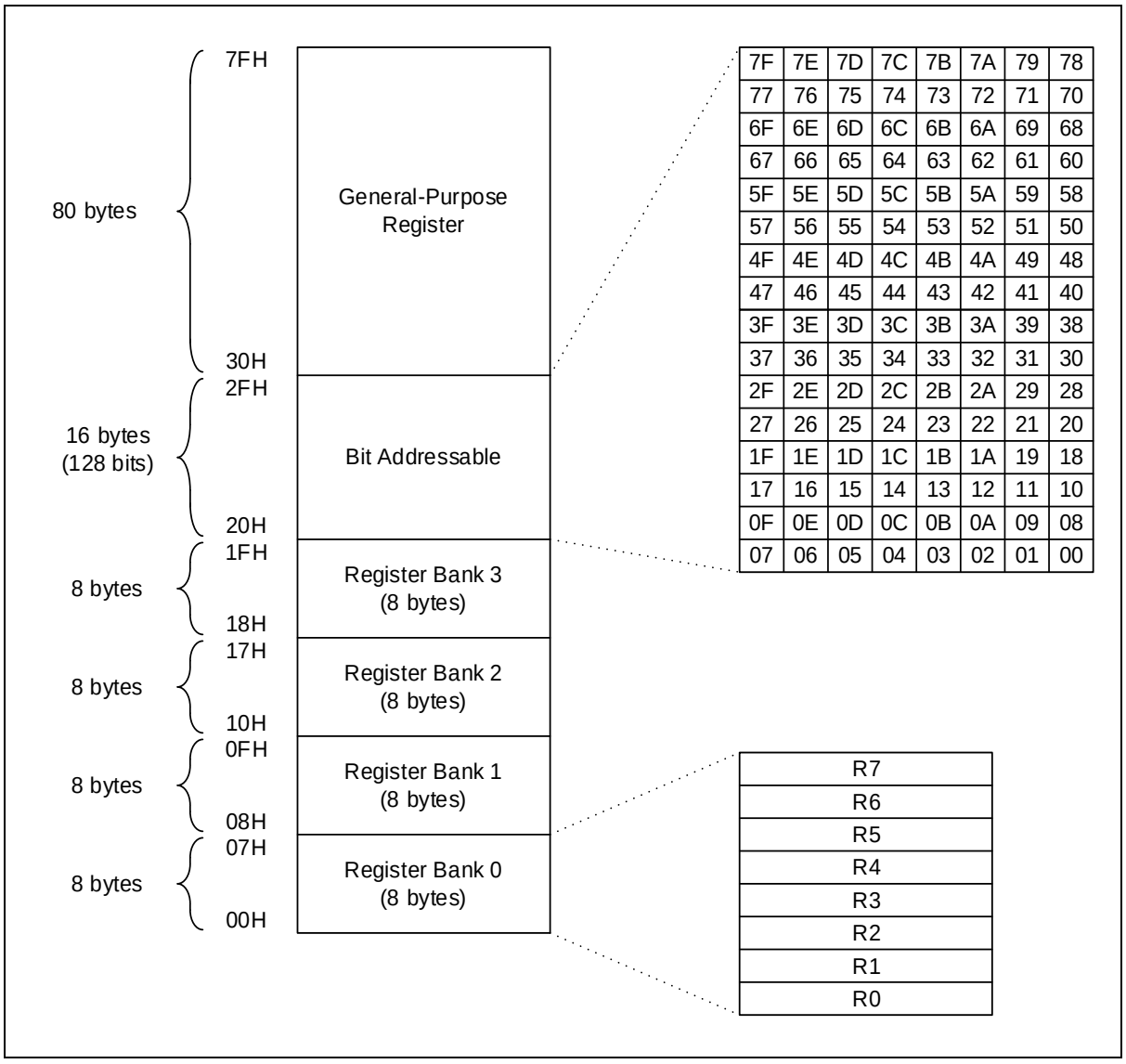



The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 6. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051-instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

Entire bytes in the lower 128 bytes can be accessed by either direct or indirect addressing, while the upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for data RAM and stack.

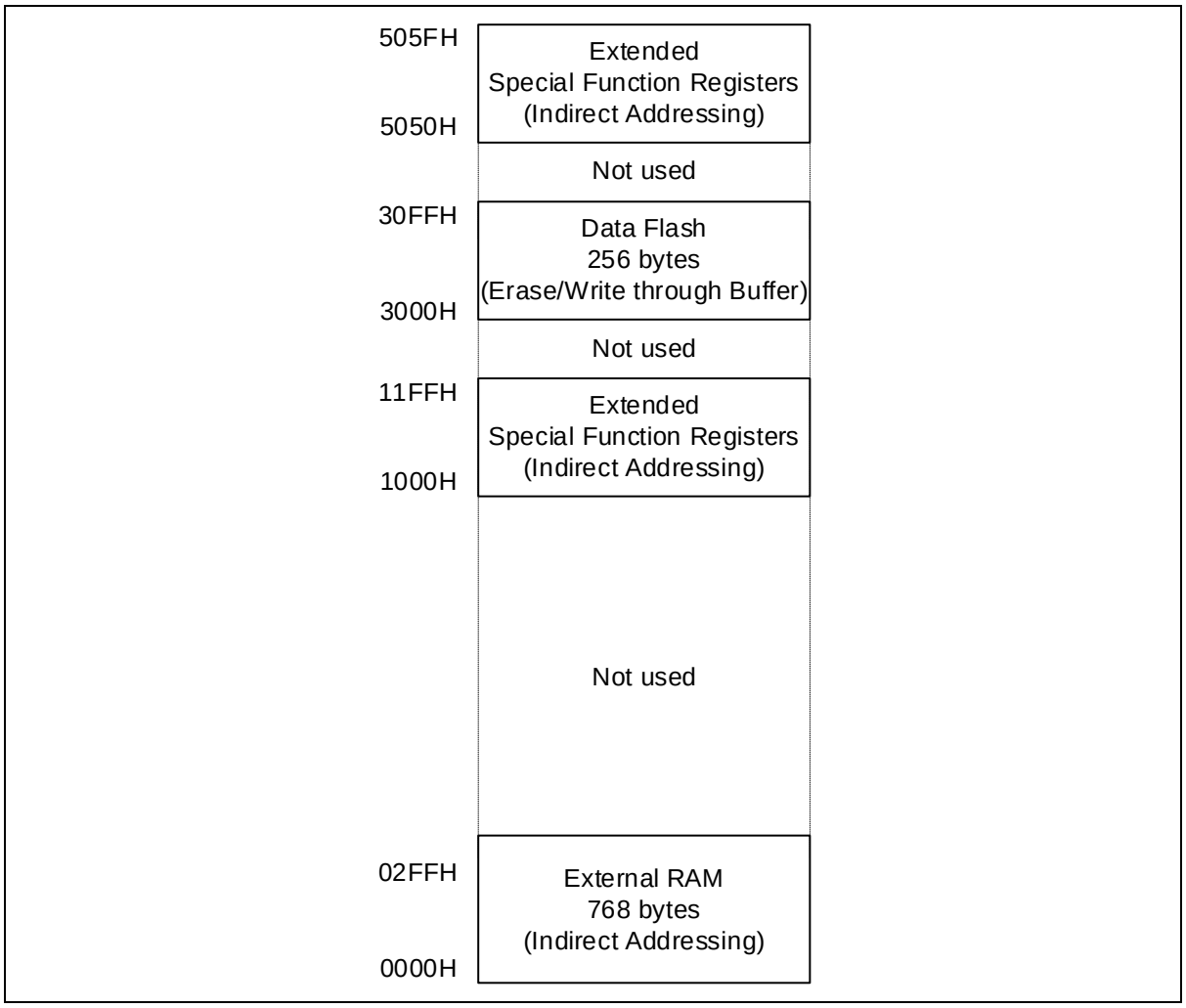
**Figure 6. Lower 128 bytes Internal RAM**



#### 2.4.2.3 Extended SFR and Data Memory Area

A96L116 has 768 bytes XRAM and 528 bytes XSFR registers. Extended SFR area has no relation with RAM nor flash memory. This area can be read or written to by using SFR in 8-bit unit.

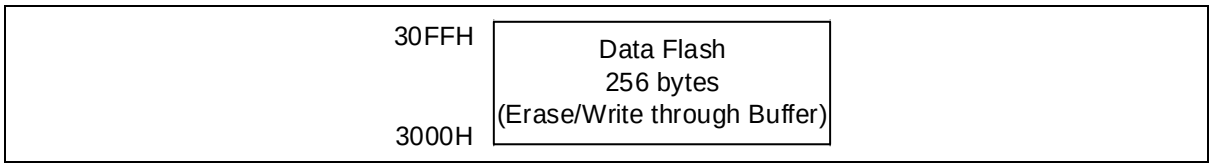
**Figure 7. Extended SFR (XSFR) Area**



#### 2.4.2.4 Data Flash Memory Area

Data flash memory is located on the extended memory area and can be read using DPTR. Data flash area can be erased or written to through the page buffer with relevant SFR.

**Figure 8. Data Flash Memory Area**




For the detailed information about Data flash, see chapter 2.4.19 Data Flash Memory.

### 2.4.3 Ports

#### 2.4.3.1 I/O Ports

A96L116 has three groups of I/O ports: P0, P1, and P2. Using SFR register, each port can be configured as an input, an output, or with an internal pull-up and open-drain type according to system configurations and design requirements.

#### 2.4.3.2 Port Description of P0

As an 8-bit I/O port, P0 controls the following registers:

- P0 data register (P0)
- P0 direction register (P0IOH/P0IOL)
- P0 debounce enable register (P0DB)
- P0 pull-up resistor selection register (P0PU)
- P0 open-drain selection register (P0OD)
- P0 Function selection registers (P0FSRH/P0FSRL)

#### 2.4.3.3 Port Description of P1

As a 6-bit I/O port, P1 controls the following registers:

- P1 data register (P1)
- P1 direction register (P1IOH/P1IOL)
- P1 pull-up resistor selection register (P1PU)
- P1 debounce enable register (P1DB)
- P1 open-drain selection register (P1OD)
- P1 Function selection registers (P1FSRH/P1FSRL)

#### 2.4.3.4 Port Description of P2

As a 4-bit I/O port, P2 controls the following registers:

- P2 data register (P2)
- P2 direction register (P2IOL)
- P2 pull-up resistor selection register (P2PU)
- P2 open-drain selection register (P2OD)
- P2 Function selection registers (P2FSRL)

### 2.4.4 Interrupt Controller

A96L116 has an interrupt controller with 15 interrupt sources, each with four priorities. All interrupt sources can be enabled or disabled individually by software except for the non-maskable interrupt that is always enabled with the highest priority and cannot be masked by software.

The interrupt controller features the followings:

- Receives requests from 15 interrupt sources.
- Six group priorities
- Four priority levels
- Multi-interrupt possibility
- If requests of different priority levels are received simultaneously, a request with higher priority level is served first.
- Each interrupt source can be controlled by an EA bit and an IEx bit.
- Interrupt latency varies ranging from three to nine machine cycles in a single interrupt system.

Non-maskable interrupt is always enabled, while maskable interrupts can be enabled through four pairs of interrupt enable registers (IE, IE1, IE2, and IE3). Each bit of the four registers can individually enable or disable a particular interrupt source. Especially bit 7 (EA) in the register IE provides overall control. It must be set to ‘1’ to enable interrupts as described in the followings:

- When EA is set to ‘0’ ➔ all interrupts are disabled.
- When EA is set to ‘1’ ➔ a particular interrupt can be individually enabled or disabled by the associate bit of the interrupt enable registers.

If an interrupt has occurred, the EA bit is automatically cleared to '0', and Program Count jumps to the interrupt service vector. The EA bit will be set to ‘1’ when executing the RETI instruction at the end of interrupt routine. Since A96L116’s interrupt controller has four-level priority, and each maskable interrupt is set to a priority level according to IP and IP1.

**Figure 9. Interrupt Group Priority Level**

| Interrupt Group | Highest → Lowest | | | |
|---|---|---|---|---|
| 0 (Bit0) | Interrupt 0 | Interrupt 6 | Interrupt 12 | Interrupt 18 |
| 1 (Bit1) | Interrupt 1 | Interrupt 7 | Interrupt 13 | Interrupt 19 |
| 2 (Bit2) | Interrupt 2 | Interrupt 8 | Interrupt 14 | Interrupt 20 |
| 3 (Bit3) | Interrupt 3 | Interrupt 9 | Interrupt 15 | Interrupt 21 |
| 4 (Bit4) | Interrupt 4 | Interrupt 10 | Interrupt 16 | Interrupt 22 |
| 5 (Bit5) | Interrupt 5 | Interrupt 11 | Interrupt 17 | Interrupt 23 |

Highest

Lowest

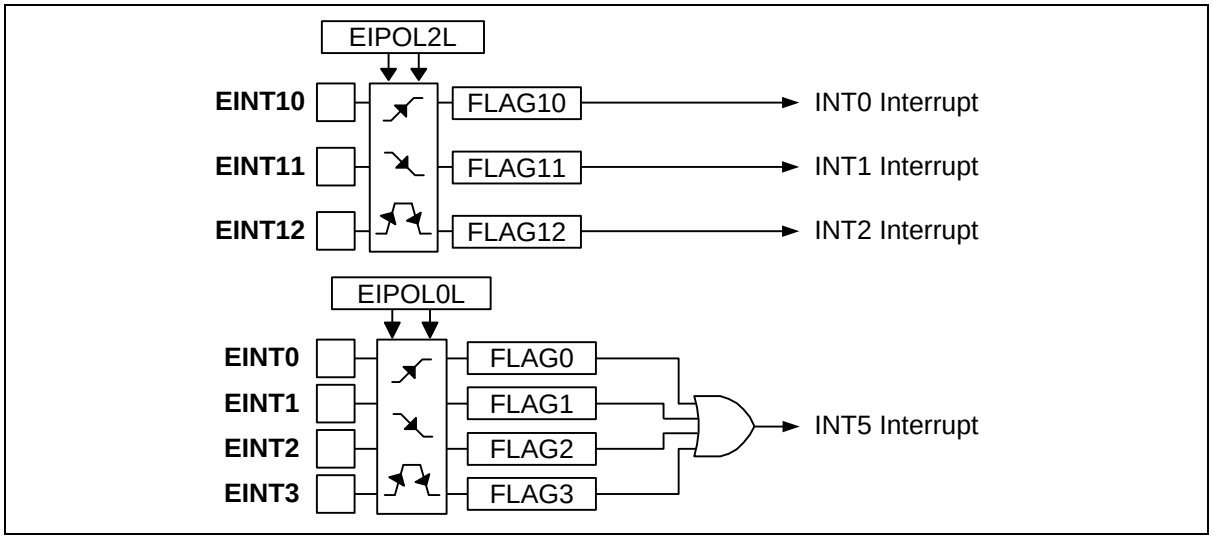
Figure 9 describes interrupt groups and their priority levels that is available for sharing interrupt priority. Priority of a group is set by two bits of Interrupt Priority (IP) registers: one bit from IP and another one bit from IP1.

Interrupt Service Routine serves an interrupt having higher priority first. If two requests of different priority levels are received simultaneously, the request with higher priority level is served prior to the lower one.

#### 2.4.4.1 External Interrupt

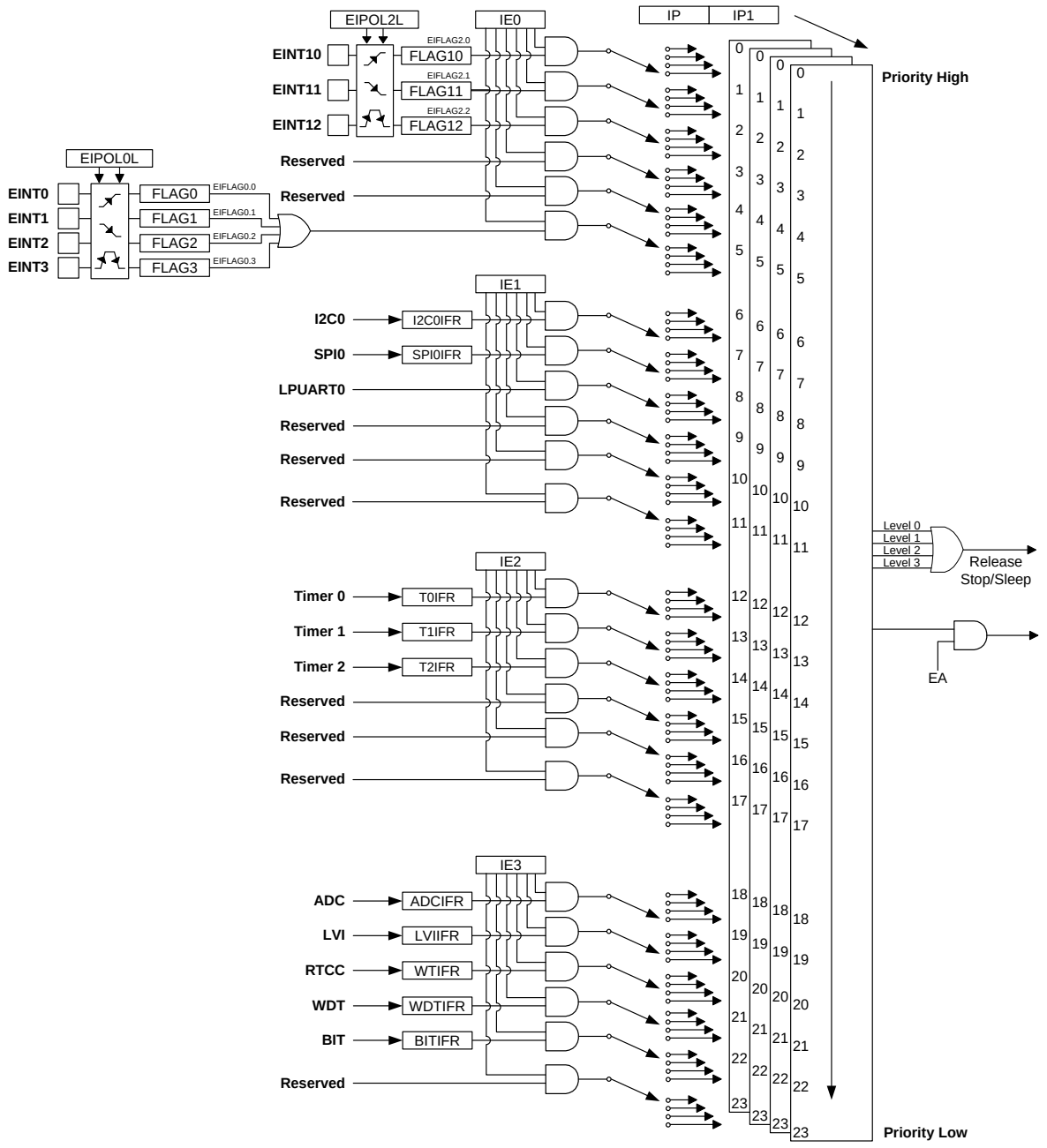
External interrupts on pins of INT0 to INT5 receive various interrupt requests in accordance with the external interrupt polarity 0 register (EIPOL0L) and external interrupt polarity 2 register (EIPOL2L) as shown in Figure 10. Each external interrupt source has enable/disable bits. An external interrupt flag register (EIFLAG) provides the status of the external interrupts.

**Figure 10. External Interrupt Description**



### 2.4.4.2 Interrupt Controller Block Diagram

**Figure 11. Interrupt Controller Block Diagram**




**NOTES:**

1. The release signal may be generated by all interrupt sources which are enabled without reference to the priority level.
2. An interrupt request is delayed while data are written to IE, IE1, IE2, IE3, IP, IP1, and PCON register.

In Figure 11, release signal for STOP and IDLE mode can be generated by all interrupt sources which are enabled without reference to priority level. An interrupt request will be delayed while data is written to one of the registers IE, IE1, IE2, IE3, IP, IP1, and PCON.

#### 2.4.4.3 Interrupt Vector Table

When a certain interrupt occurs, a LCALL (Long Call) instruction pushes the contents of the PC (Program Counter) onto the stack and loads the appropriate vector address. CPU pauses from its current task for some time and processes the interrupt at the vector address.

The Interrupt controller supports 24 interrupt sources, and each interrupt source has a determined priority order as shown in Table 5.

**Table 5. Interrupt Vector Address Table**

| Interrupt Source | Symbol | Interrupt Enable Bit | Priority | Mask | Vector Address |
|---|---|---|---|---|---|
| Hardware RESET | RESETB | - | 0 | Non-Maskable | 0000H |
| External Interrupt 10 | INT0 | IE.0 | 1 | Maskable | 0003H |
| External Interrupt 11 | INT1 | IE.1 | 2 | Maskable | 000BH |
| External Interrupt 12 | INT2 | IE.2 | 3 | Maskable | 0013H |
| – | INT3 | IE.3 | 4 | Maskable | 001BH |
| – | INT4 | IE.4 | 5 | Maskable | 0023H |
| External Interrupt 0 – 3 | INT5 | IE.5 | 6 | Maskable | 002BH |
| I2C0 Interrupt | INT6 | IE1.0 | 7 | Maskable | 0033H |
| SPI0 Interrupt | INT7 | IE1.1 | 8 | Maskable | 003BH |
| LPUART0 Interrupt | INT8 | IE1.2 | 9 | Maskable | 0043H |
| – | INT9 | IE1.3 | 10 | Maskable | 004BH |
| – | INT10 | IE1.4 | 11 | Maskable | 0053H |
| – | INT11 | IE1.5 | 12 | Maskable | 005BH |
| T0 Match Interrupt | INT12 | IE2.0 | 13 | Maskable | 0063H |
| T1 Match Interrupt | INT13 | IE2.1 | 14 | Maskable | 006BH |
| T2 Match Interrupt | INT14 | IE2.2 | 15 | Maskable | 0073H |
| – | INT15 | IE2.3 | 16 | Maskable | 007BH |
| – | INT16 | IE2.4 | 17 | Maskable | 0083H |
| – | INT17 | IE2.5 | 18 | Maskable | 008BH |
| ADC Interrupt | INT18 | IE3.0 | 19 | Maskable | 0093H |
| LVI Interrupt | INT19 | IE3.1 | 20 | Maskable | 009BH |
| RTCC Interrupt | INT20 | IE3.2 | 21 | Maskable | 00A3H |
| WDT Interrupt | INT21 | IE3.3 | 22 | Maskable | 00ABH |
| BIT Interrupt | INT22 | IE3.4 | 23 | Maskable | 00B3H |
| – | INT23 | IE3.5 | 24 | Maskable | 00BBH |

To execute the maskable interrupts, both EA bit and a corresponding bit of IEx associated with a specific interrupt source must be set to ‘1’. When an interrupt request is received, a particular interrupt request flag is set to ‘1’ and maintains its status until CPU accepts the interrupt. After the interrupt acceptance, the interrupt request flag will be cleared automatically.

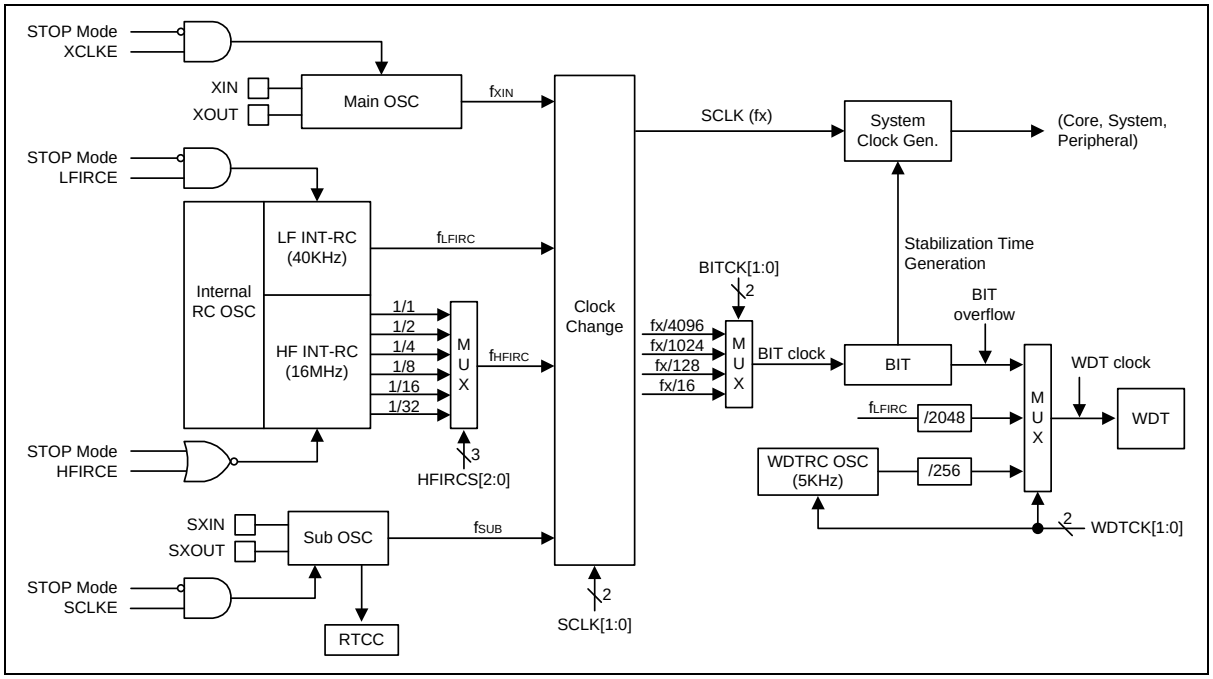
### 2.4.5 Clock Generator

As shown in Figure 12, a clock generator produces basic clock pulses which provide a CPU and peripherals with a system clock. The default system clock is a 1 MHz HF INT-RC oscillator and default division rate is sixteen. To stabilize the system internally, it is used 1 MHz HF INT-RC oscillator on POR.

A96L116 incorporates three types of oscillators:

- Calibrated HF Internal RC Oscillator (16 MHz)
  - HF INT-RC OSC/32 (0.5 MHz)
  - HF INT-RC OSC/16 (1 MHz, default system clock)
  - HF INT-RC OSC/8 (2 MHz)
  - HF INT-RC OSC/4 (4 MHz)
  - HF INT-RC OSC/2 (8 MHz)
  - HF INT-RC OSC/1 (16 MHz)
- Internal WDTRC Oscillator (5 kHz)
- LF INT-RC Oscillator (40 kHz)

**Figure 12. Clock Generator in Block Diagram**



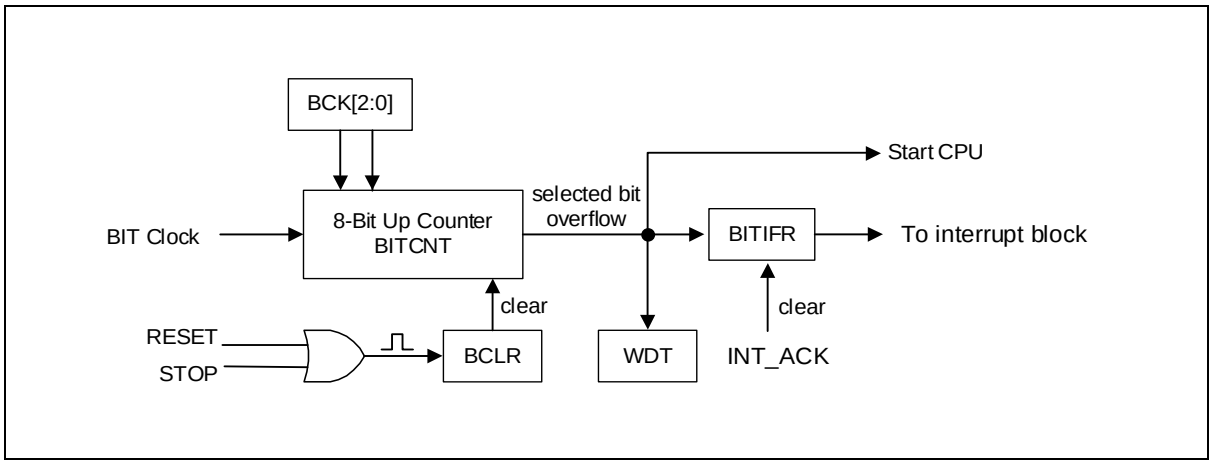
### 2.4.6 Basic Interval Timer (BIT)

A96L116 has a free running 8-bit Basic Interval Timer (BIT). BIT generates the time base for watchdog timer counting and provides a basic interval timer interrupt (BITIFR).

BIT of A96L116 features the followings:

- During Power On, BIT gives a stable clock generation time.
- On exiting Stop mode, BIT gives a stable clock generation time.
- As a timer, BIT generates a timer interrupt.

**Figure 13. Basic Interval Timer in Block Diagram**



### 2.4.7 WatchDog Timer (WDT)

Watchdog Timer (WDT) is used to rapidly detect CPU malfunctions such as endless looping caused by noise. In addition, it is used to resume the CPU in a normal state. Watchdog timer signal for malfunction detection can be used as either a CPU reset or an interrupt request. When the WDT is not being used for the detection of the CPU malfunctions, it can be used as a timer generating an interrupt at fixed intervals.

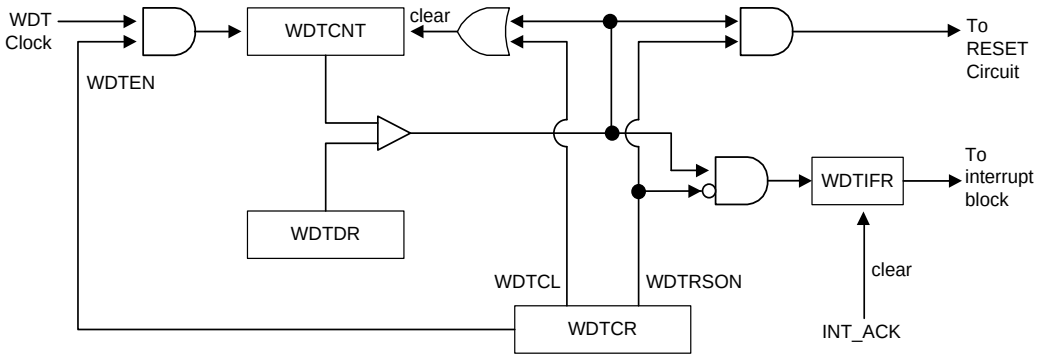
The WDT can be used in a free running 8-bit timer mode or in a watch dog timer mode by setting WDTRSON bit, which is WDTCR[6]. If '1' is written to WDTCR[5], WDT counter value is cleared and counts up. After 1 machine cycle, this bit is cleared to '0' automatically.

The WDT consists of an 8-bit binary counter and a watchdog timer data register. When the value of an 8-bit binary counter is equal to the 8 bits of WDTCNT, an interrupt request flag is generated. This can be used as a watchdog timer interrupt or a reset of CPU in accordance with a bit WDTRSON.

The input clock source of watch dog timer is BIT overflow and WDTRC. The interval of watchdog timer interrupt is decided by the BIT overflow period and WDTDR set value. Equation of the WDT interrupt interval is described in the followings:

- WDT Interrupt Interval = (BIT Interrupt Interval) × (WDTDR Value + 1)
- WDT Interrupt Interval = 2048 / $f_{LFIRC}$ × (WDTDR Value + 1) when LFIRC
- WDT Interrupt Interval = 256 / $f_{WDTRC}$ × (WDTDR Value + 1) when WDTRC

**Figure 14. Watchdog Timer in Block Diagram**




**NOTE:**

1. Watchdog timer clock depends on WDTCK[1:0] bits in WDTCR register.

### 2.4.8 Real Timer Clock and Calendar (RTCC)

The Real Timer Clock and Calendar (RTCC) has a function for RTC (Real Time Clock) and calendar operations.

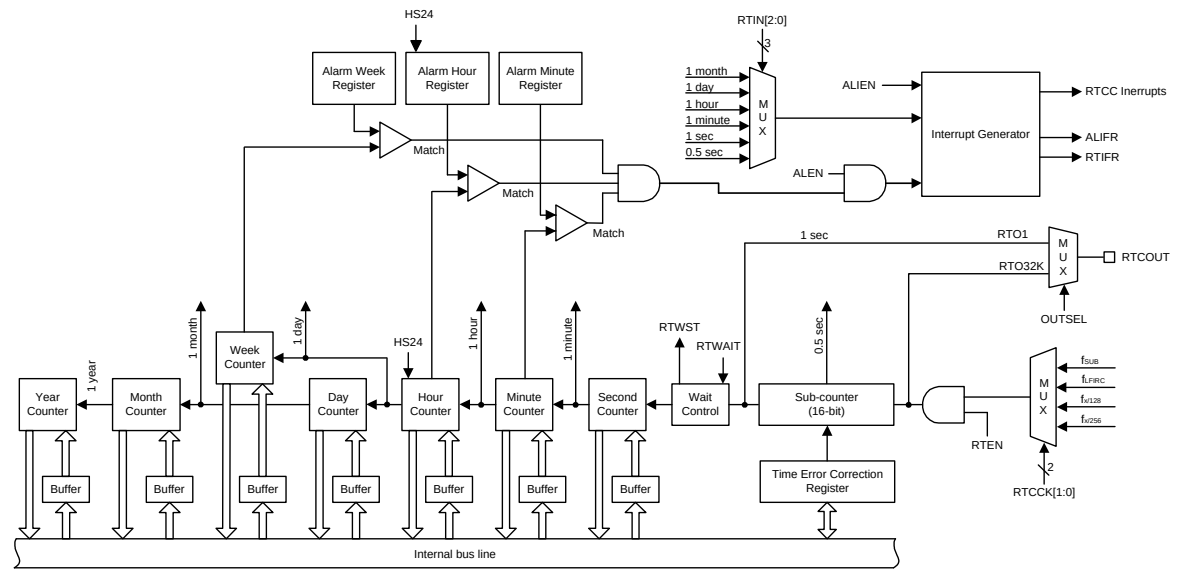
The internal structure of the RTCC is implemented with the clock source select circuit, second/minute/hour/day/week/month/year counter circuits, alarm circuit, output select circuit, and error correction circuit.

The RTCC is an independent BCD counter.

The main operations of the RTCC include the followings:

- Calendar counting 0.5 seconds, seconds, minutes, hours, days, weeks, months, and years up to the year 2099.
- Time error correction function
- Alarm function with interrupt
- Wake-up possibility from STOP mode

**Figure 15. RTCC Block Diagram**




**NOTE:**

1. Time in the block diagram is based on 32.768 kHz

### 2.4.9 16-bit Timer (T0)

TIMER0 is a 16-bit Timer, which has a multiplexer and eight registers such as Timer0 A Data Register High/Low, Timer0 B Data Register High/Low, Timer0 Capture Data Register High/Low, and Timer 0 Control Register High/Low (T0ADRH, T0ADRL, T0BDRH, T0BDRL, T0CAPH, T0CAPL, T0CRH, T0CRL).

TIMER0 operates in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into Input Capture Data Register (T0CAPH/T0CAPL) by the EINT10 event and the edge of $f_{SUB}$ clock or $f_{LFIRC}$ clock. T0 outputs the comparison result between counter and data register through T0O port in timer/counter mode, and outputs PWM waveform through PWM0O port in the PPG mode.

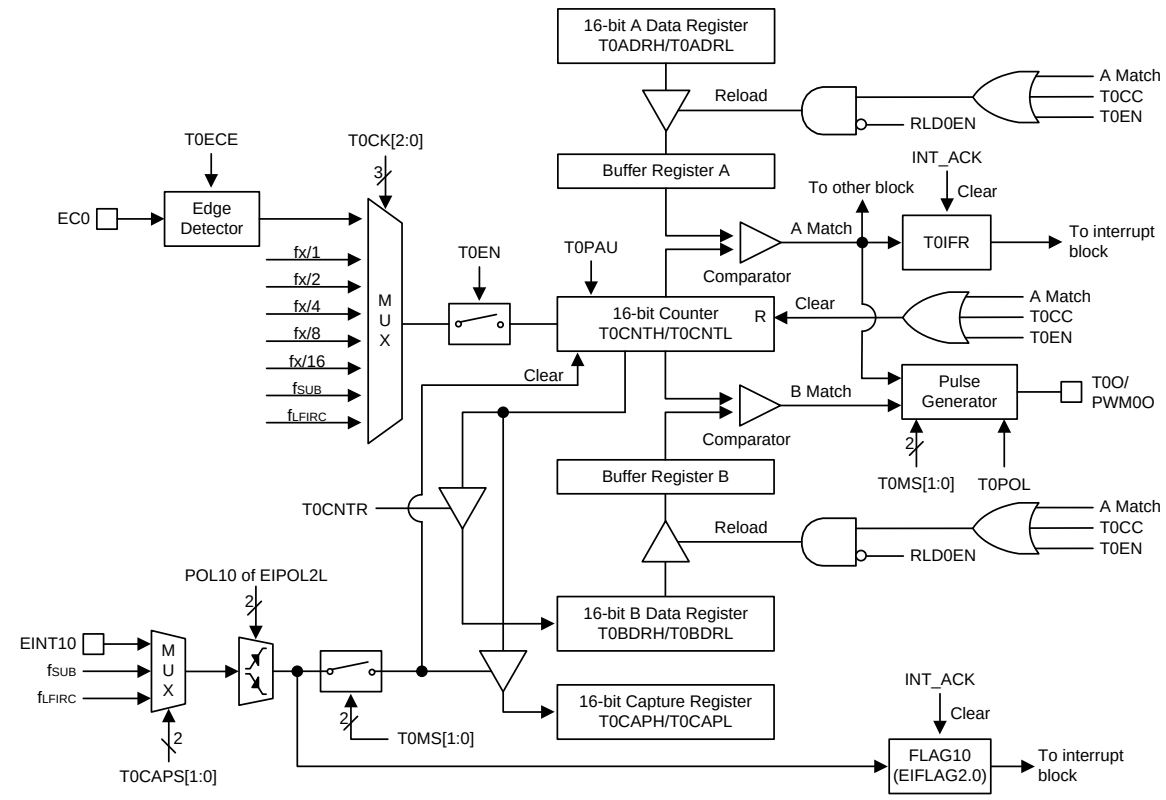
T0 uses an internal clock or an external clock (EC0, $f_{SUB}$, $f_{LFIRC}$) as an input clock source. The available clock sources are listed below, and one is selected by clock selection bits (T0CK[2:0]).

- Timer 0 clock sources: $f_X$/1, 2, 4, 8, 16, $f_{SUB}$, $f_{LFIRC}$, and EC0

**Table 6. TIMER0 Operating Modes**

| T0EN | P0FSRL[4] | T0MS[1:0] | T0CK[2:0] | Timer 0 |
|---|---|---|---|---|
| 1 | 1 | 00 | XXX | 16-bit Timer/Counter Mode |
| 1 | 0 | 01 | XXX | 16-bit Capture Mode |
| 1 | 1 | 10 | XXX | 16-bit PPG Mode (one-shot mode) |
| 1 | 1 | 11 | XXX | 16-bit PPG Mode (repeat mode) |

**Figure 16. 16-bit Timer 0 in Block Diagram**




**NOTES:**

1. T0EN is automatically cleared to logic ‘0’ after one pulse is generated at a PPG one-shot mode.
2. RLD0EN bit must be ‘0’ when T0EN bit is changed from ‘0’ to ‘1’.

### 2.4.10 16-bit Timer (T1/T2)

T1 and T2 are 16-bit timers, and each timer has a multiplexer and eight registers such as Timer A Data Register High/Low, Timer B Data Register High/Low, Capture Data Register High/Low, and Control Register High/Low (TnADRH, TnADRL, TnBDRH, TnBDRL, TnCAPH, TnCAPL, TnCRH, TnCRL).

T1 and T2 operate in one of four operating modes:

- 16-bit capture mode
- 16-bit timer/ counter mode
- 16-bit PPG output mode (one-shot mode)
- 16-bit PPG output mode (repeat mode)

Specifically in capture mode, data is captured into Input Capture Data Register (TnCAPH/TnCAPL) by incorporating with EINT1n event. Timer1 and Timer2 output the comparison result between counter and data register through TnO port in timer/counter mode. Timer1 and Timer2 output PWM wave form through PWMnO port in the PPG mode).

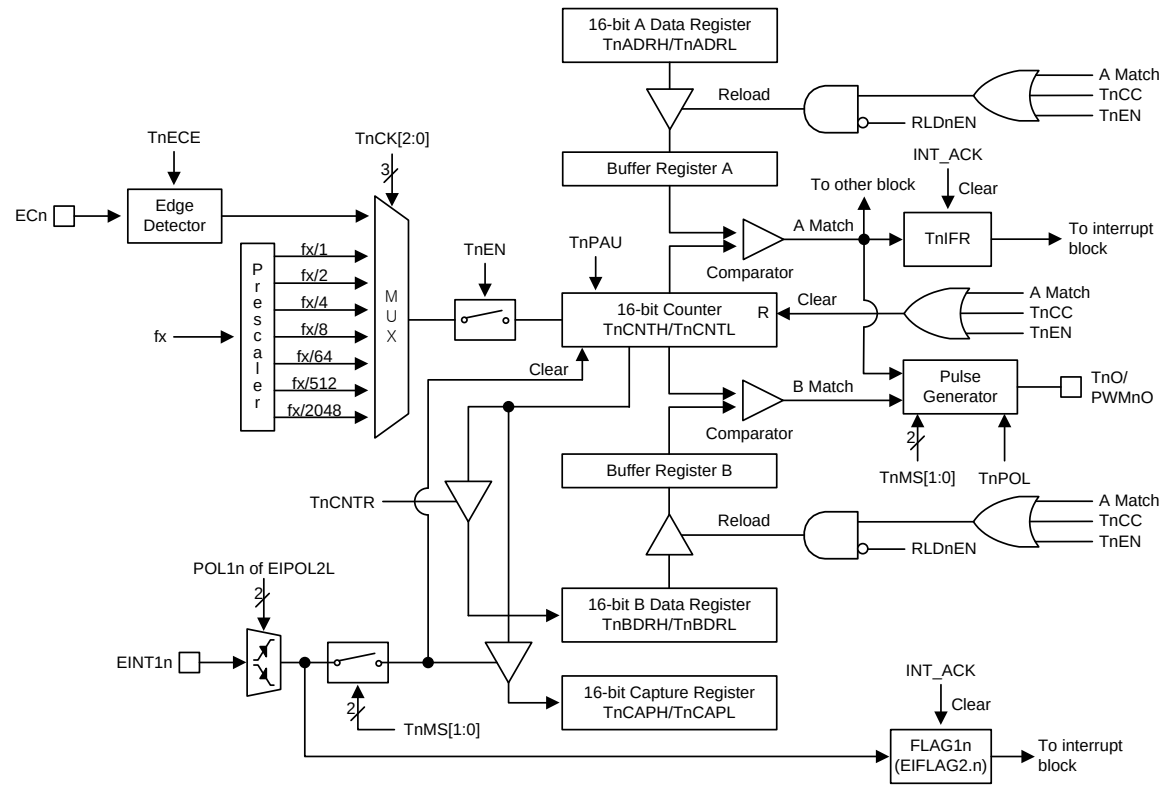
Timer1 and Timer2 use an internal clock or an external clock (ECn) as an input clock source. The clock sources are described below, and one is selected by clock selection logic which is controlled by clock selection bits (TnCK[2:0]).

- Timer1 and Timer2 clock sources: $f_X$ / 1, 2, 4, 8, 64, 512, 2048 and ECn

**Table 7. Timer1 and Timer2 Operating Modes**

| TnEN | P0FSRL[6] (T1)/ P1FSRL[6] (T2) | TnMS[1:0] | TnCK[2:0] | Timer n |
|---|---|---|---|---|
| 1 | 1/0 | 00 | XXX | 16 Bit Timer/Counter Mode |
| 1 | 0/0 | 01 | XXX | 16 Bit Capture Mode |
| 1 | 1/0 | 10 | XXX | 16 Bit PPG Mode (one-shot mode) |
| 1 | 1/0 | 11 | XXX | 16 Bit PPG Mode (repeat mode) |

**Figure 17. 16-bit Timer n in Block Diagram (n = 1 and 2)**




**NOTES:**

1. TnEN is automatically cleared to logic ‘0’ after one pulse is generated at a PPG one-shot mode.
2. RLDnEN bit must be ‘0’ when TnEN bit is changed from ‘0’ to ‘1’.

### 2.4.11 12-bit A/D Converter

Analog-to-digital (A/D) converter converts an analog input signal to a corresponding 12-bit digital output value. The A/D converter module has a multiplexer that switches eight analog inputs to the A/D converter's input.

The A/D converter module also has two pairs of registers – A/D Converter Control Register and Data Register. These registers have the functions of selecting the input channel, controlling the conversion state, and holding the value of the conversion result for the corresponding channel.

**Figure 18. 12-bit ADC Block Diagram**

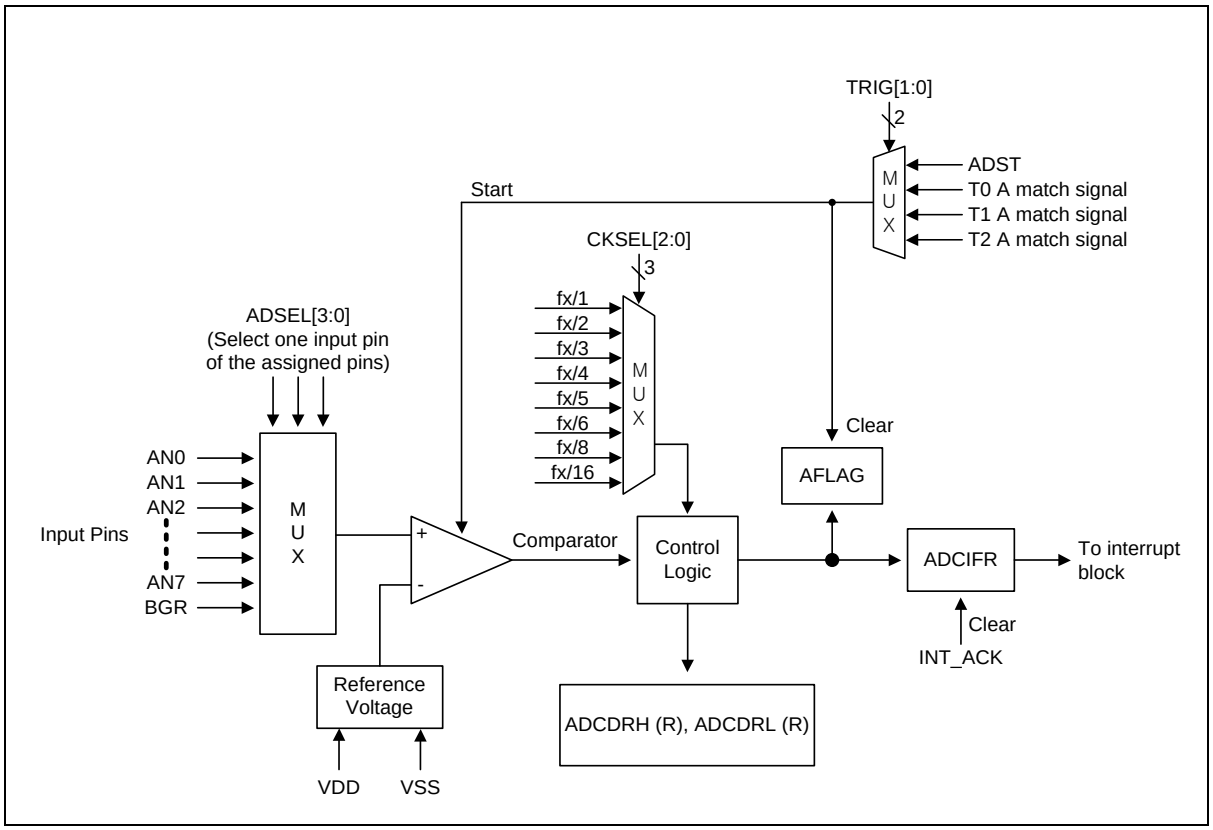
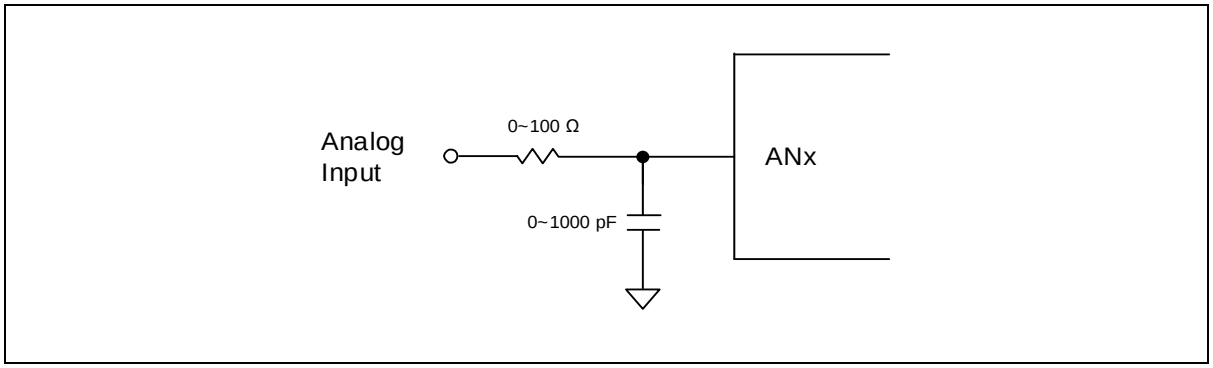



**Figure 19. AD Analog Input Pin with Capacitor**



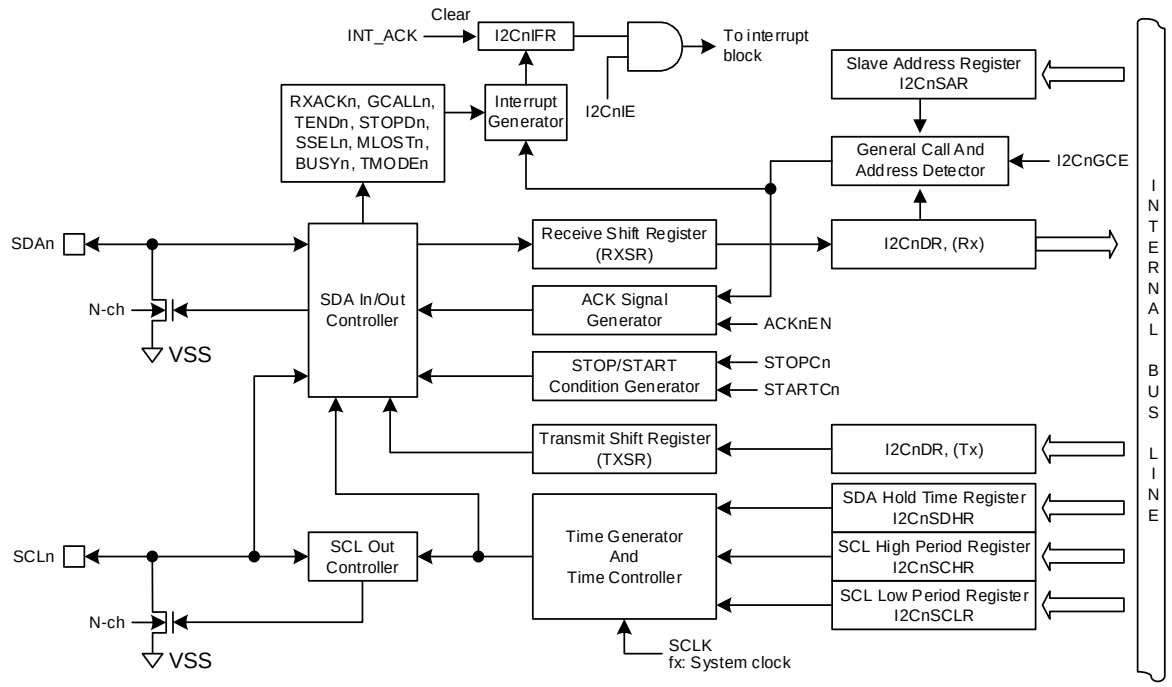
### 2.4.12 Inter-Integrated Circuit (I2C) Interface

The I2C is the industrial standard serial communication protocol, which uses two bus lines, Serial Data Line (SDA) and Serial Clock Line (SCL), to exchange data. Because both SDAn and SCLn lines are open-drain output, each line needs a pull-up resistor.

The features of built-in I2C are listed below.

- Compatible with the I2C bus standard
- Multi-master operation
- Up to 400 kHz data transfer speed
- 7-bit slave address
- Support two slave addresses
- Both master and slave operations
- Bus busy detection

**Figure 20. I2C Block Diagram (n = 0)**



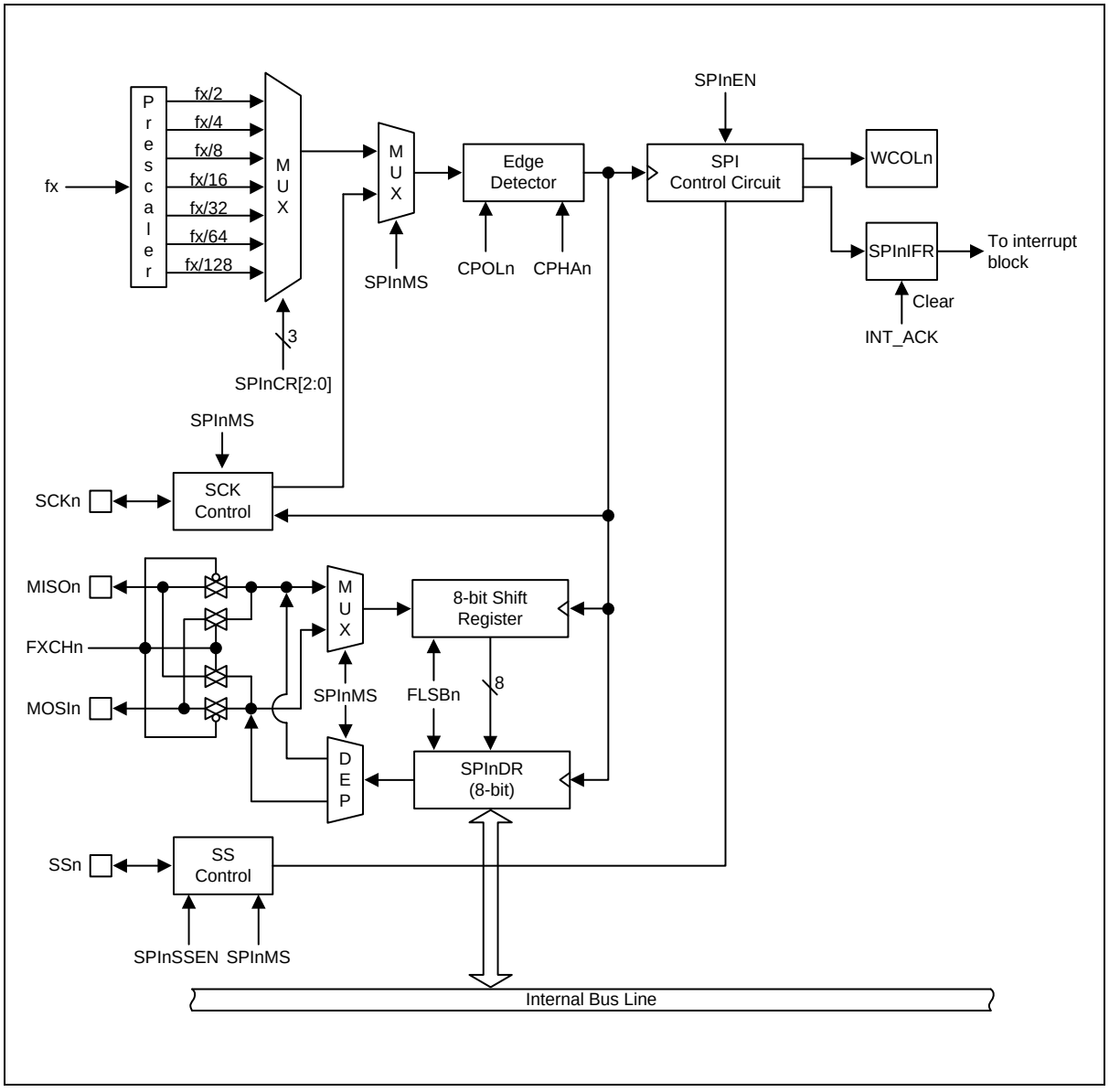

**NOTE:**

1. When the corresponding port of I2Cn is a sub-function for SCLn/SDAn pin, the SCLn/SDAn pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

### 2.4.13 Serial Peripheral Interface (SPI)

A96L116 has one channel of Serial Peripheral Interface (SPI). The SPI operates synchronous serial data transfer with an external device. Built-in SPI supports full-duplex communication by four-wire (MOSIn, MISOn, SCKn, SSn), and also supports master and slave mode with configurable polarity, phase of serial clock (SCKn), and bit transfer order (MSB or LSB).

**Figure 21. SPI Block Diagram (n = 0)**



### 2.4.14 Low Power UART (LPUART)

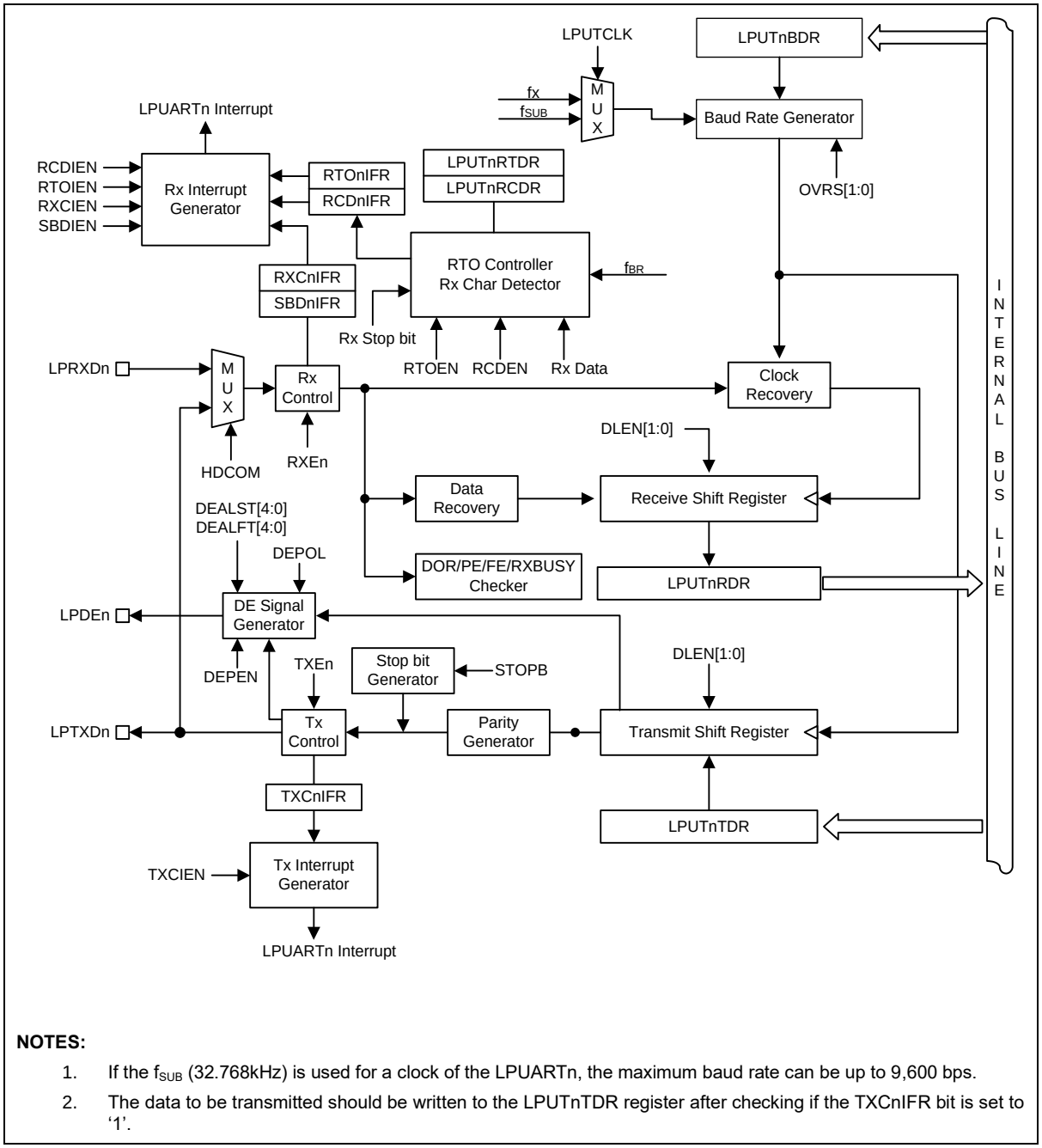
The A96L116 has one channel of built-in Low-Power UART (Universal Asynchronous Receiver / Transmitter) module.

LPUART supports asynchronous serial communication up to 9,600 bps with a 32.768 kHz sub-oscillator even when the core is in STOP mode. LPUART also supports one-wire half-duplex communications.

The features of built-in LPUART are listed below.

- Full-duplex and half-duplex operations
- Built-in baud rate generator
- Supports serial frames with 5,6,7, or 8 data bits and 1 or 2 stop bits
- Odd or even parity generation, and parity check supported by hardware
- Supports receive character detection and receive time out function
- Baud rate compensation function
- Supports up to 9,600 bps with 32.768 kHz sub-oscillator
- Data Overrun detection
- Framing error detection
- Double-speed asynchronous communication mode

**Figure 22. LPUART Block Diagram (n = 0)**




**NOTES:**

1. If the $f_{SUB}$ (32.768kHz) is used for a clock of the LPUARTn, the maximum baud rate can be up to 9,600 bps.
2. The data to be transmitted should be written to the LPUTnTDR register after checking if the TXCnIFR bit is set to '1'.

### 2.4.15 Flash Memory CRC and Checksum Generator

Flash Memory CRC (Cyclic Redundancy Check) generator of A96L116 generates 16-bit CRC code bits from flash and a generator polynomial. The CRC code for each input data frame is appended to the frame.

Specifically, CRC-based technique is used to verify data transmission or storage integrity. In the scope of the functional safety standards, this technique offers a means of verifying the Flash memory integrity. The flash CRC generator helps compute a signature of software during runtime, to be compared with a reference signature.

The CRC generator has the following features:

- Auto CRC and User CRC Mode
- CRC Clock: $f_{HFIRC}$, $f_{HFIRC}/2$, $f_{HFIRC}/4$, $f_{HFIRC}/8$ and fx (System clock)
- CRC-16 polynomial: 0x8C81 ($X^{16} + X^{15} + X^{11} + X^{10} + X^7 + 1$)

**Figure 23. CRC-16 Polynomial Structure**

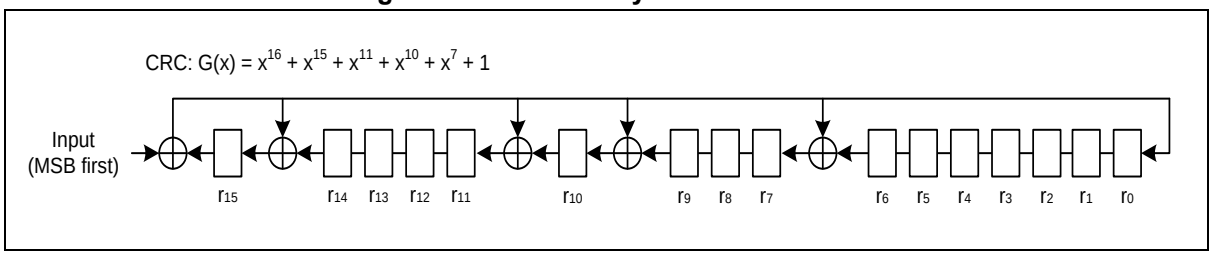
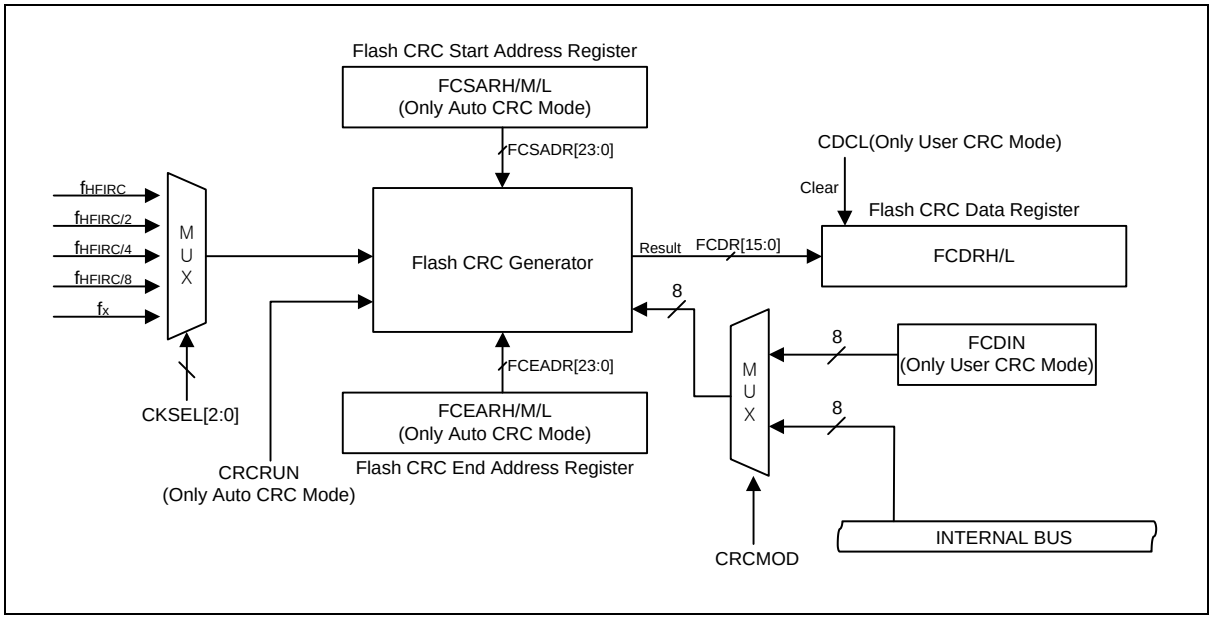



**Figure 24. Flash CRC/Checksum Generator Block Diagram**



### 2.4.16 Power-Down Operation

A96L116 offers two power-down modes to minimize energy consumption: IDLE mode and STOP mode. In the IDLE or STOP mode, the core is stopped, and power consumption is reduced considerably.

#### 2.4.16.1 Peripheral Operation in IDLE / STOP Mode

Table 8. Peripheral Operation during Power-down Mode describes the operations of internal peripherals during IDLE mode and STOP mode.

**Table 8. Peripheral Operation during Power-down Mode**

| Peripheral | IDLE mode | STOP mode |
|---|---|---|
| CPU | All CPU operations are disable | All CPU operations are disable |
| RAM | Retain | Retain |
| Basic Interval Timer | Operates continuously | Stop |
| Watchdog Timer | Operates continuously | Stop (Can be operated with WDTRC and LFIRC) |
| Timer 0 | Operates continuously | Halted (Only when the Event Counter Mode is Enabled or when $f_{SUB}$/$f_{LFIRC}$ is selected for the clock of timer 0, Timer 0 operates Normally) |
| Timer 1 2 | Operates continuously | Halted (Only when the Event Counter Mode is Enabled, Timer operates Normally) |
| RTCC | Operates continuously | Can be operated with $f_{SUB}$ |
| ADC | Operates continuously | Stop |
| LPUART | Operates continuously | Can be operated with $f_{SUB}$ |
| I2C | Operates continuously | Only operate with external clock |
| SPI | Operates continuously | Only operate with external clock |
| HF-Internal OSC | Oscillation | Stop |
| LF-Internal OSC | Oscillation | Can be operated with setting value |
| WDTRC OSC (5KHz) | Can be operated with setting value | Can be operated with setting value |
| I/O port | Retain | Retain |
| Control register | Retain | Retain |
| Address data bus | Retain | Retain |
| Release method | By RESET, all Interrupts | By RESET, Timer 0, Timer Interrupt (EC1, EC2), External Interrupt, WDT, LPUART, RTCC |

### 2.4.17 Reset

When a reset event occurs, the core and on-chip peripherals are to be initialized, and the internal registers of the core and the peripherals will be initialized with the reset value. Table 9 shows the reset values of internal registers.

**Table 9. Reset Values of Internal Registers**

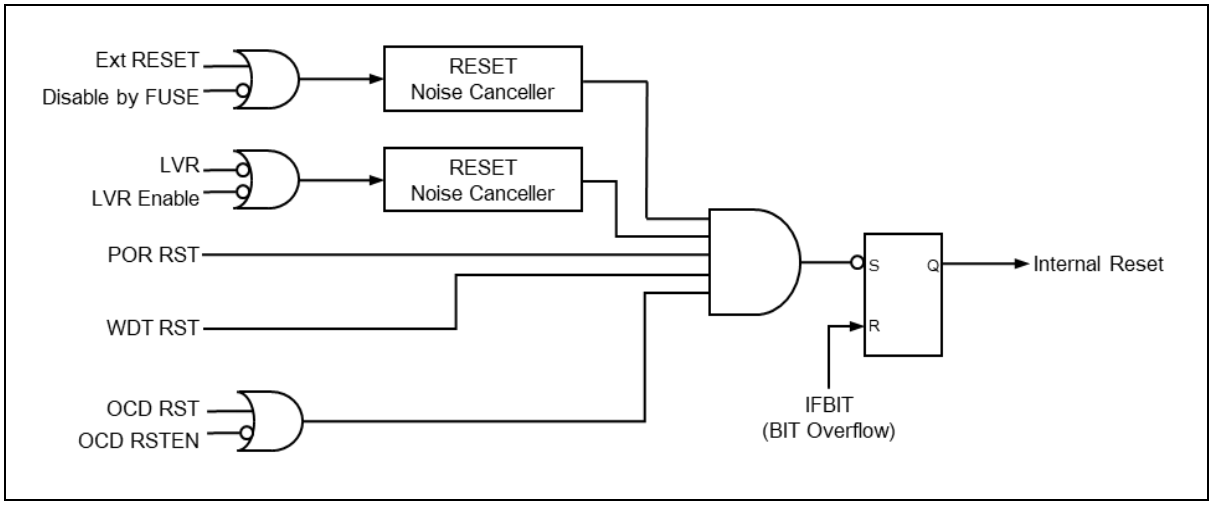
| Internal Register | Reset Value |
|---|---|
| Program Counter (PC) | 0000H |
| Accumulator | 00H |
| Stack Pointer (SP) | 07H |
| Peripheral clock | On |
| Control register | Refer to peripheral registers. |

A96L116 has five reset sources listed below:

- External RESETB Input
- Power-on Reset (POR)
- WDT Overflow Reset (in the case of WDTEN='1')
- Low Voltage Reset (in the case of LVREN='0')
- OCD Reset

Figure 25 shows the reset block of A96L116.

**Figure 25. Reset Block Diagram**



### 2.4.18 Flash Memory

A96L116 has 16 KB on-chip flash memory, which is used as program memory. On-chip flash memory supports writing and erasing features through self-program mode and OCD (On-Chip Debug) program mode. The flash memory can be read by ‘MOVC’ instruction and programmed in OCD, serial ISP mode or user program mode.

Flash memory has the following features:

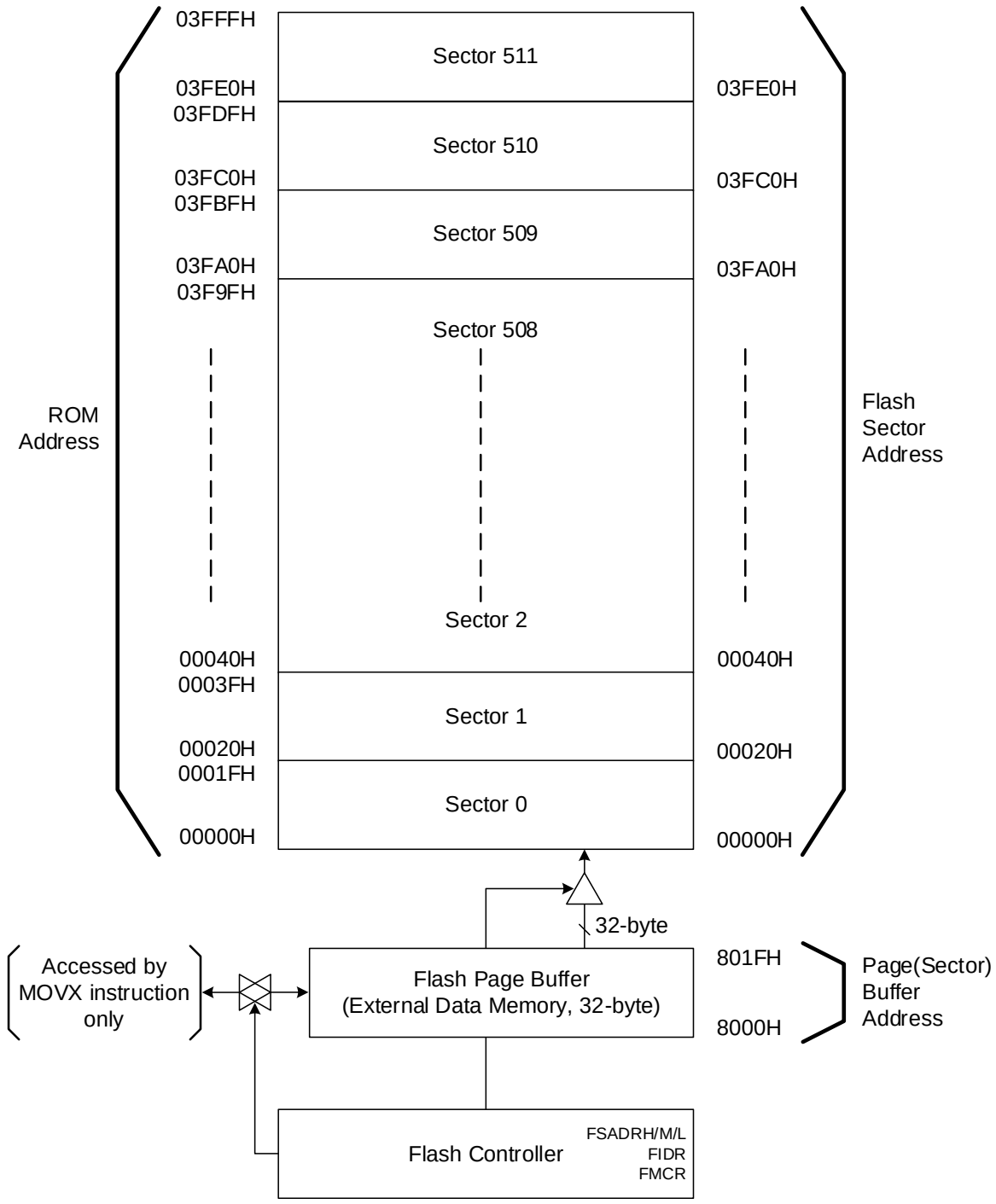
- Size of flash memory: 16 Kbytes
- Built-in program/erase voltage generation
- Supports self-program mode and OCD mode program/erase
- Up to 10,000 program/erase cycles at typical voltage and temperature for flash memory

**NOTE:**

1. The RXE0 bit of LPUT0CR1 register should be disabled before flash memory erase and write start.

#### 2.4.18.1 Flash Program ROM Structure

**Figure 26. Flash Program ROM Structure**




**NOTES:**

1. The flash memory doesn't support byte erase mode.
2. The flash shouldn't be entered in erase/write mode during data flash program.
   So before the flash program start, the data flash busy bit (DFMBUSY) should be checked whether the bit is '1' or not. If the bit is '1', do not start flash program.

### 2.4.19 Data Flash Memory

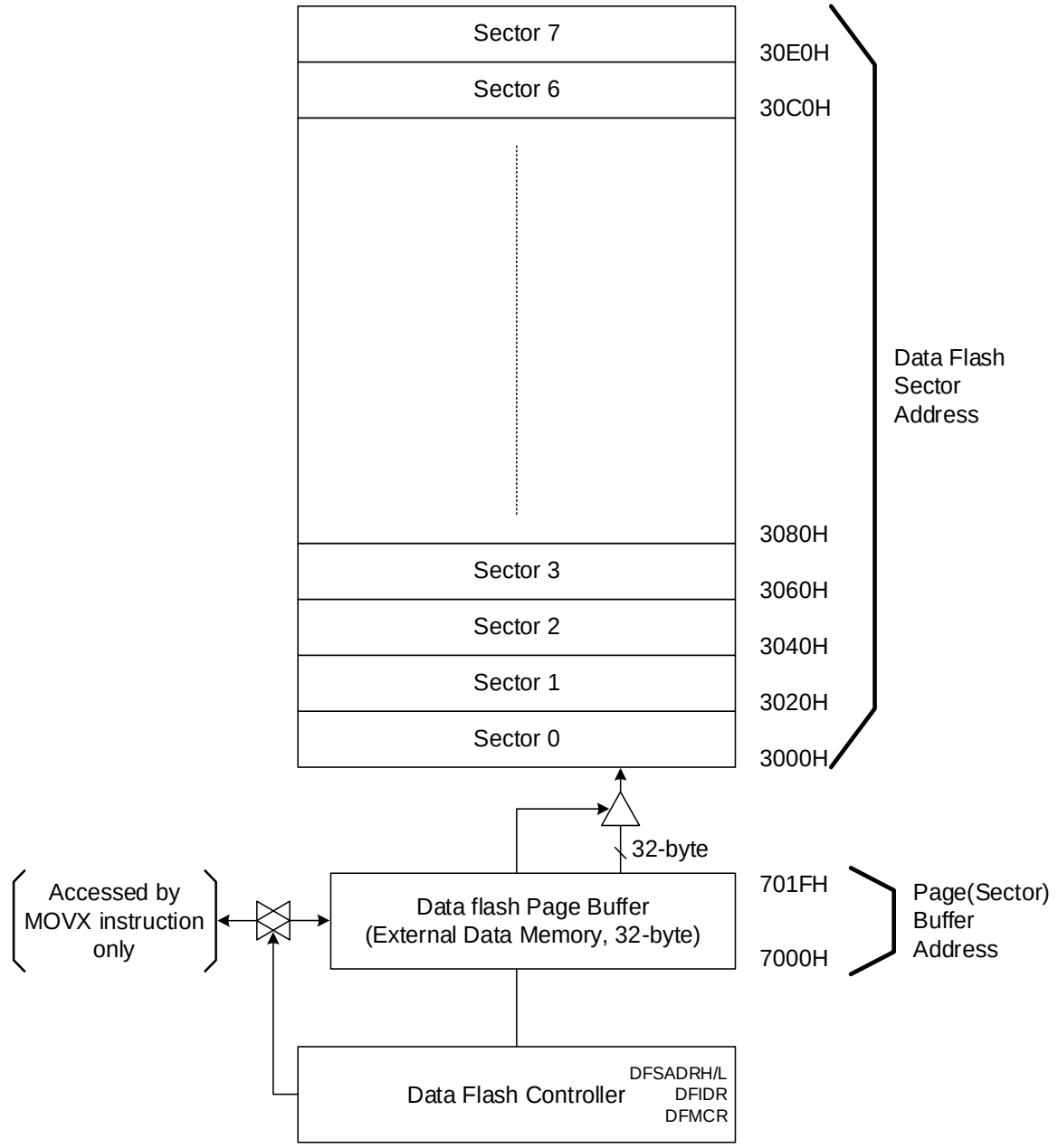
The A96L116 has 256 bytes of on-chip data flash memory with self-programming and erasing capabilities. The data flash memory can be read by ‘MOVX’ instruction.

- Size of data flash memory: 256 bytes
- Built-in program/erase voltage generation
- Supports self-program mode and OCD mode program/erase.
- Up to 100,000 program/erase cycles at typical voltage and temperature for memory

The endurance of the write and erase cycles of the internal data flash memory can be increased significantly with strategic usage such as dividing smaller unit size recycling. When dividing 256 bytes into eight blocks with 32 bytes, each block is used up to 100,000 cycles, and then the total erase and write will be 800,000 cycles.

Figure 27 shows the block diagram of the data flash memory with page buffer, data flash controller, and the sector addresses.

**Figure 27. Data Flash Structure**




**NOTES:**

1. The data flash memory doesn't support byte erase mode.
2. The data flash is in extended data memory area.
3. If Idle and Stop are executed on data flash erase/write, the erase/write is forcibly terminated. So before entering Idle and Stop mode, the data flash busy bit (DFMBUSY) should be checked whether the bit is '1' or not. If the bit is '1', do not enter Idle and Stop mode.

## 2.5 Development Tools

This chapter describes a wide range of development tools for A96L116. ABOV offers software tools, debuggers, and programmers to help users develop target applications. ABOV supports a set of development ecosystem for the customers.

### 2.5.1 Compiler

ABOV semiconductor does not provide any compiler for A96L116. However, since A96L116 has Mentor 8051 as its CPU core, you can use all kinds of third party's standard 8051 compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our OCD emulator and debugger. Please visit our website www.abovsemi.com for more information regarding the OCD emulator and debugger.

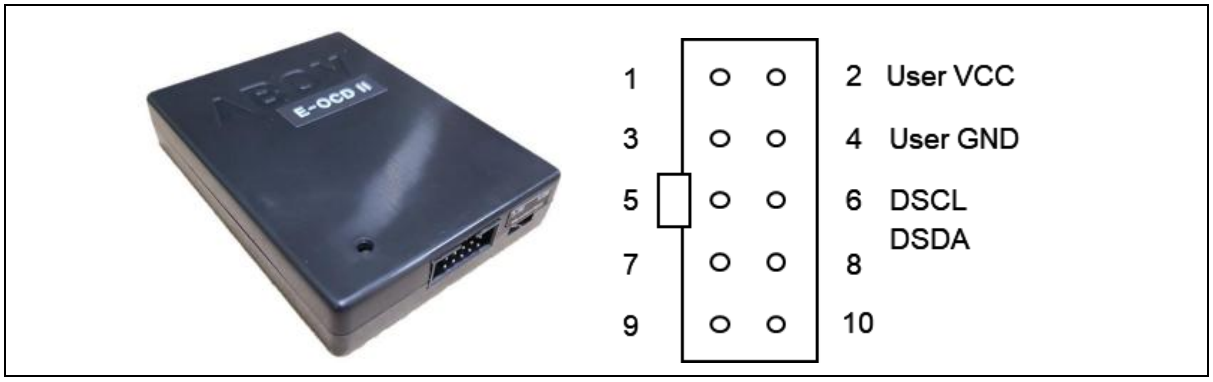
### 2.5.2 E-OCD II Interface and OCD Debugger

The E-OCD II interface supports ABOV Semiconductor's 8051 series microcontroller emulation. The E-OCD II uses two wires interfacing between host computer and microcontroller, which is attached to target system. The E-OCD II can read or change the value of microcontroller's internal memory and I/O peripherals. In addition, the E-OCD II controls microcontroller's internal debugging logic. This means E-OCD II controls emulation, step run, monitoring and many more functions regarding debugging.

The OCD debugger program runs underneath Windows Operating System such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the E-OCD II is provided in chapter 4.1.6.1 Recommended Circuit and Layout. More detailed information about the E-OCD II, please visit our website www.abovsemi.com and download the debugger software and documents.

**Figure 28. E-OCD II and OCD Pin Descriptions**




Following are the OCD mode connections:

- DSCL (A96L116 P01 port)
- DSDA (A96L116 P00 port)

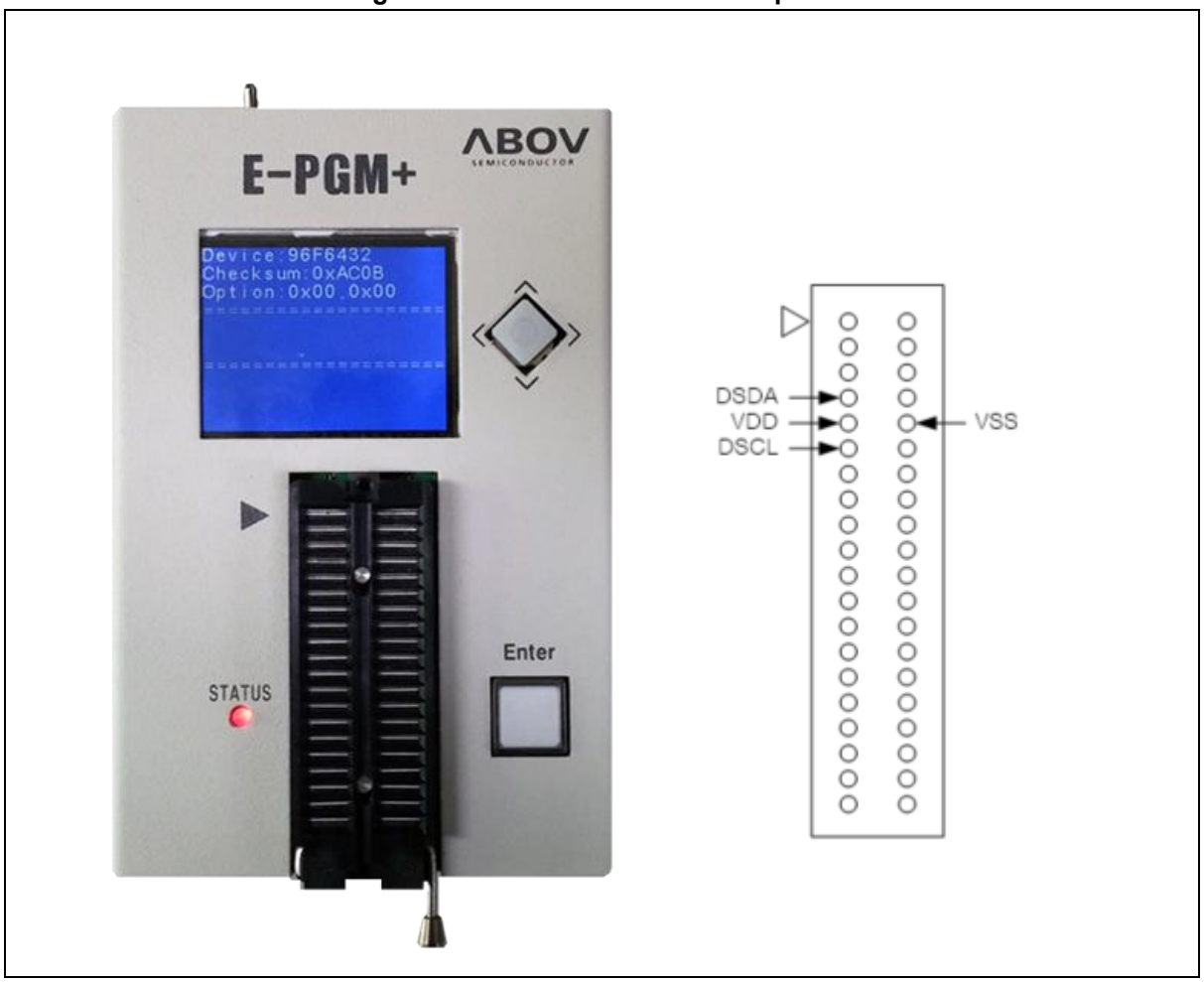
### 2.5.3 Programmer

#### 2.5.3.1 E-PGM+ and E-PGM Serial

E-PGM+ and E-PGM Serial are universal programmers and allow users to program on the device directly.

- Support all ABOV / ADAM devices
- Fast programming time with internal buffers
- TFT LCD Display

**Figure 29. E-PGM+ and Pin Descriptions**



#### 2.5.3.2 Gang Programmer

E-Gang4 and E-Gang6 allow a user to program on multiple devices at a time. They run not only in a host computer controlled mode but also in standalone mode without a host computer control. USB interface is available, and it is easy to connect to the handler.

**Table 10. Specification of E-Gang4 and E-Gang6**

| Gang programmer | E-Gang4 | E-Gang6 |
|---|---|---|
| **Dimension (x, y, h)** | 33.5 × 22.5 × 35 mm | 148.2 × 22.5 × 35 mm |
| **Weight** | 2.0 kg | 2.8 kg |
| **Input voltage** | DC Adaptor 15 V / 2 A | DC Adaptor 15 V / 2 A |
| **Operating temperature** | –10°C to +40°C | –10°C to +40°C |
| **Storage temperature** | –30°C to +80°C | –30°C to +80°C |

**Figure 30. E-Gang4 and E-Gang6 (for Mass Production)**

### 2.5.4 MTP Programming

Program memory of A96L116 is an MTP Type. This flash is accessed through four pins such as DSCL, DSDA, VDD, and VSS in serial data format. Table 11 describes each pin and corresponding I/O status.

**Table 11. Pins for MTP Programming**

| OCD Pin Name | Device Pin Name | During Programming | |
|---|---|---|---|
| | | I/O | Description |
| DSCL | P01 | I | Serial clock pin. Input only pin. |
| DSDA | P00 | I/O | Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port. |
| VDD, VSS | VDD, VSS | — | Logic power supply pin. |

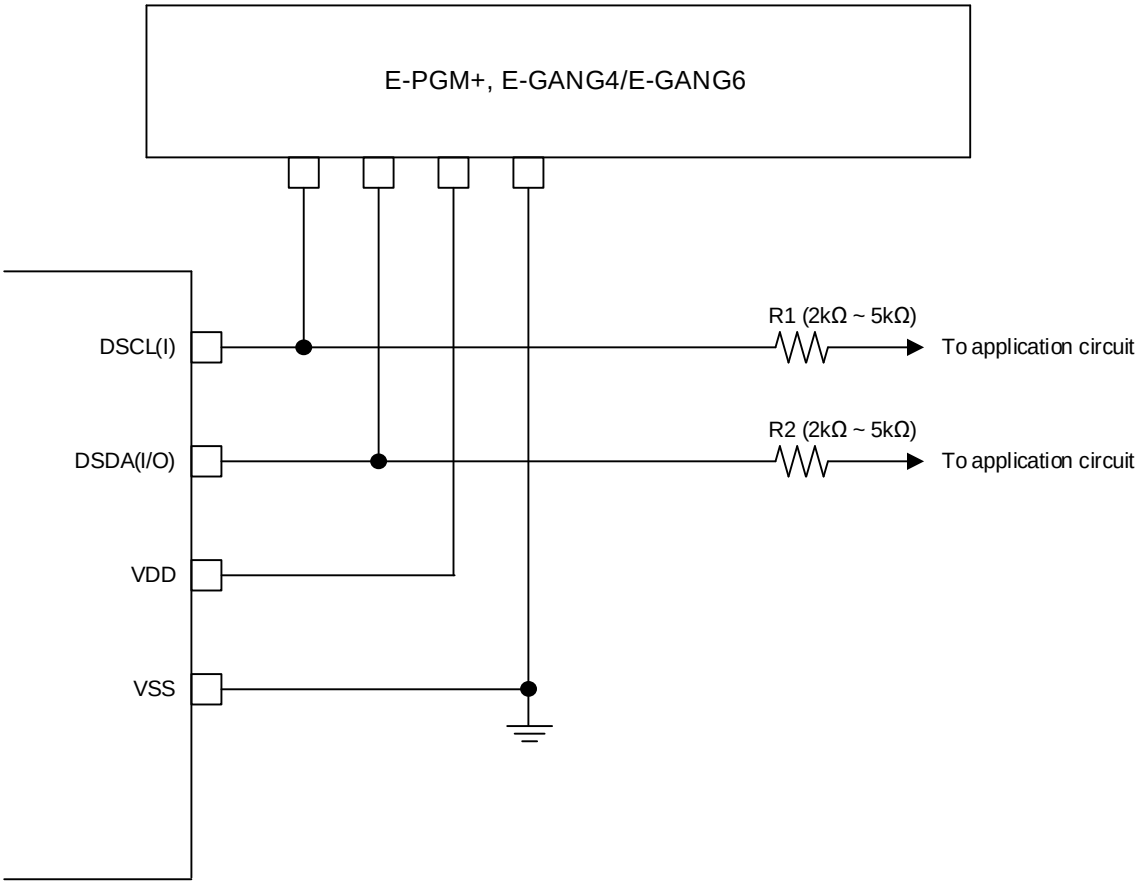
#### 2.5.4.1 On-Board Programming

The A96L116 needs only four signal lines including VDD and VSS pins for programming flash with serial protocol. Therefore, on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

### 2.5.5 Circuit Design Guide

When programming Flash memory, the programming tool needs four signal lines, DSCL, DSDA, VDD, and VSS. When you design a PCB circuit, you should consider the usage of these four signal lines for the on-board programming.

**Figure 31. PCB Design Guide for On-Board Programming**




**NOTES:**

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damage to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high-speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

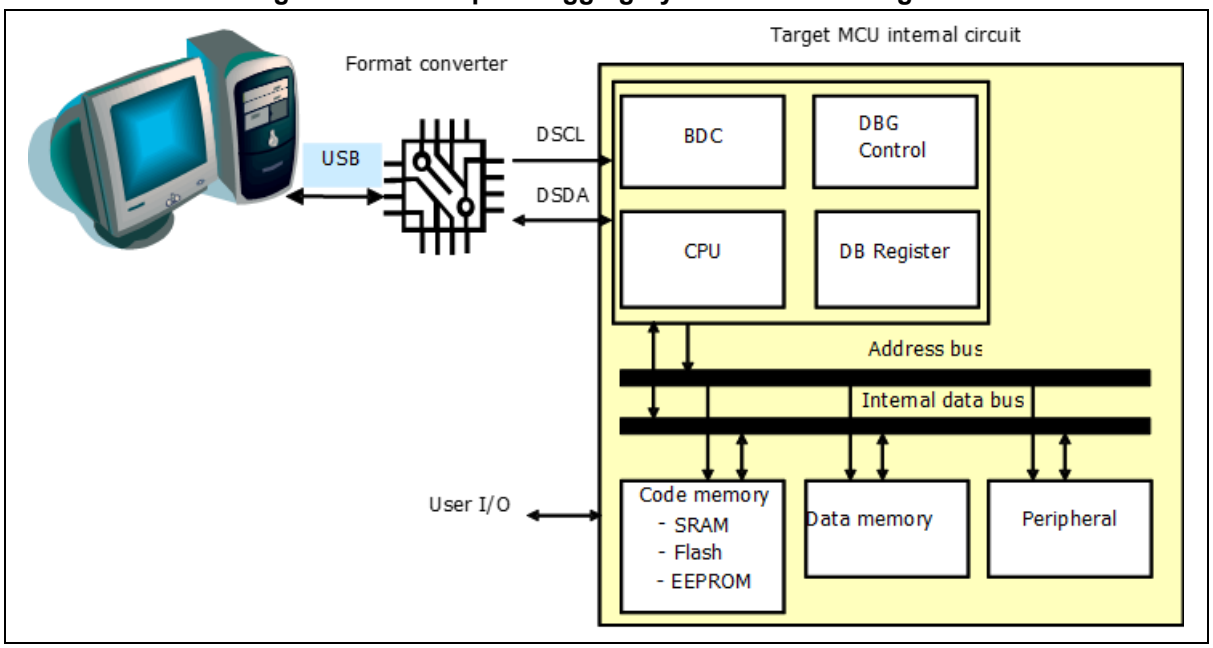
#### 2.5.5.1 On-Chip Debug System

Detail descriptions for programming via the OCD interface can be found in the following figures. Table 12 describes features of OCD and Figure 32 shows a block diagram of the OCD interface and the On-chip Debug system.

**Table 12. Features of OCD**

| | |
|---|---|
| **Two Wire External Interface** | • One serial clock input<br>• One bi-directional serial data bus |
| **Debugger Access** | • All internal peripherals<br>• Internal data RAM<br>• Program Counter<br>• Flash memory and EEPROM memory |
| **Extensive On-Chip Debugging Supports for Break Conditions** | • Break instruction<br>• Single step break<br>• Program memory break points on single address<br>• Programming of Flash, Data Flash, Fuses, and Lock bits through the two-wire interface<br>• On-Chip Debugging supported by OCD Interface |
| **Operating Frequency** | • The maximum frequency of a target microcontroller |

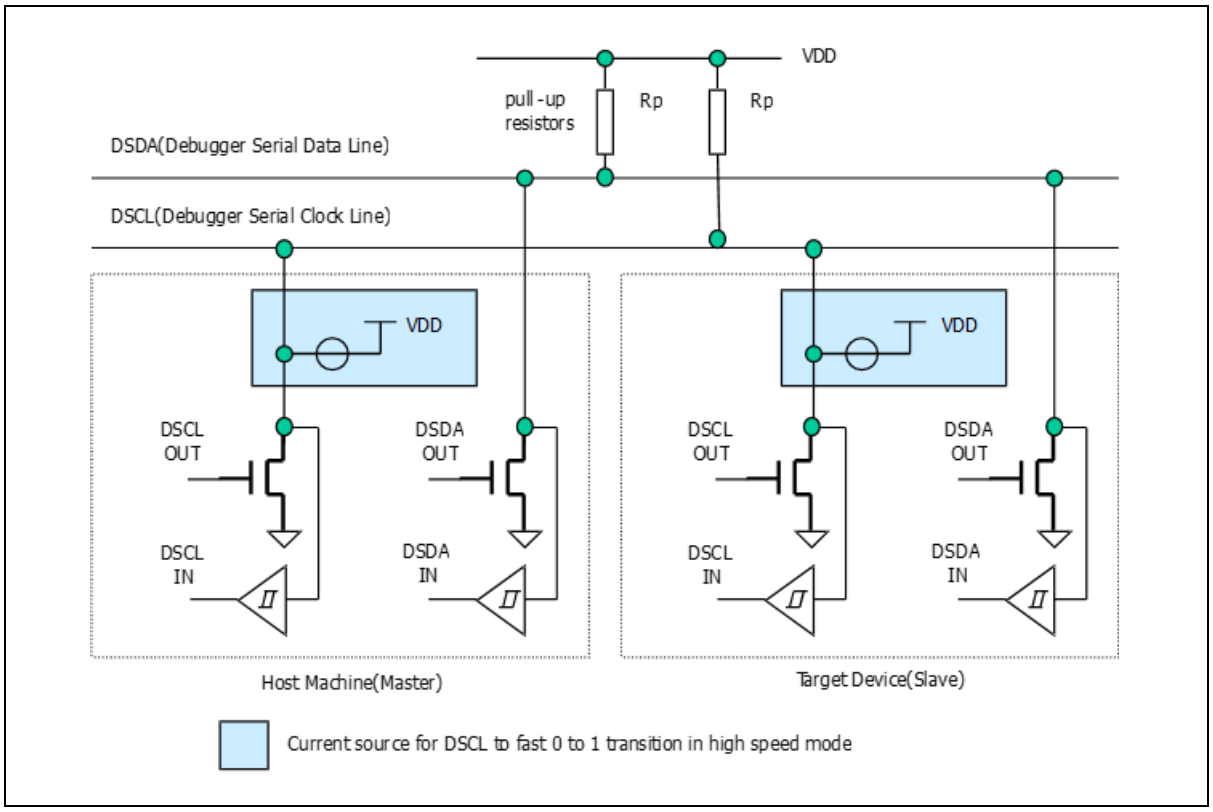
**Figure 32. On-Chip Debugging System in Block Diagram**



### 2.5.5.2 Connection of Transmission

Two-pin interface connection uses open-drain (wire-AND bidirectional I/O).

**Figure 33. Connection of Transmission**



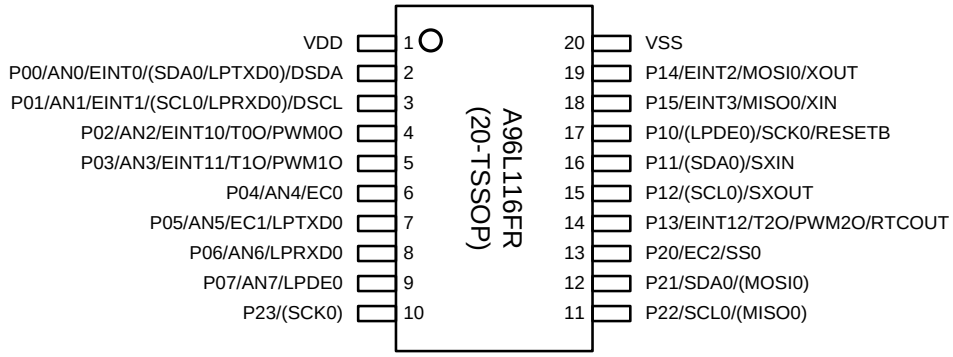
# 3. Pinouts and Pin Descriptions

In this chapter, A96L116 pinouts and pin descriptions are described.

## 3.1 Pinouts

### 3.1.1 A96L116FR (20-TSSOP)

**Figure 34. A96L116FR 20-TSSOP Pinouts**

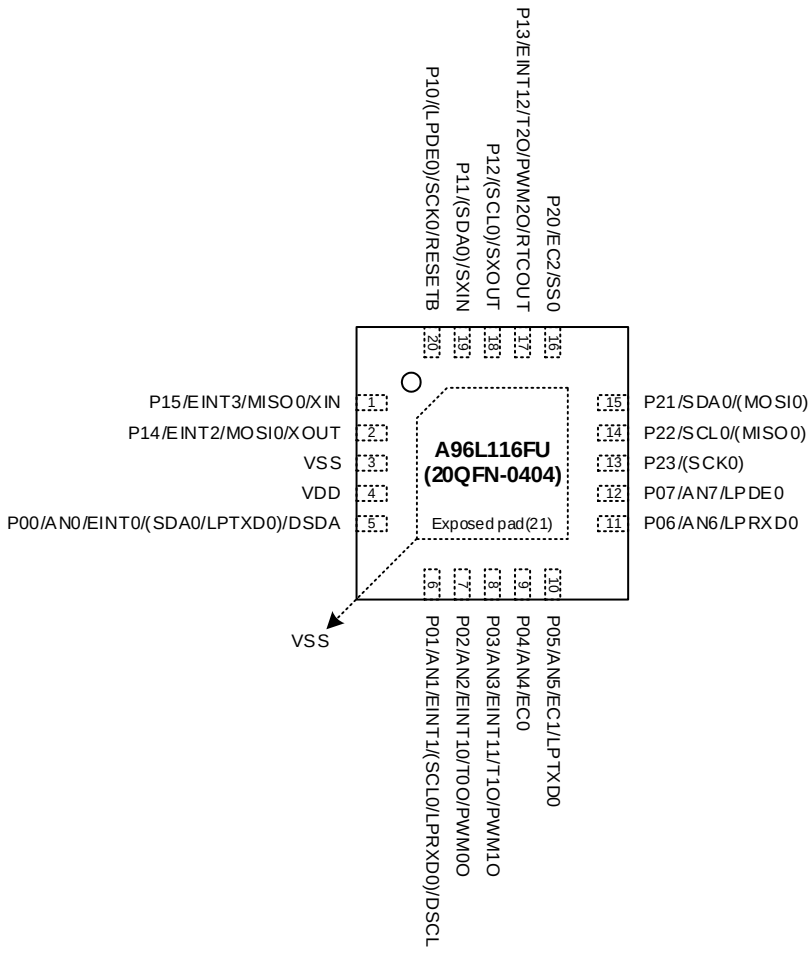



**NOTE:**

1. For the On-Chip Debugging, ISP assigns P0[1:0] pins for DSCL and DSDA respectively.

### 3.1.2 A96L116FU (20-QFN)

**Figure 35. A96L116FU 20-QFN Pinouts**

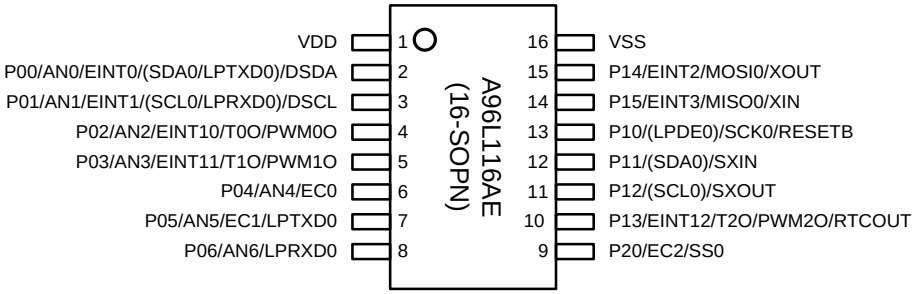



**NOTE:**

1. For the On-Chip Debugging, ISP assigns P0[1:0] pins for DSCL and DSDA respectively.

### 3.1.3 A96L116AE (16-SOPN)

**Figure 36. A96L116AE 16-SOPN Pinouts**

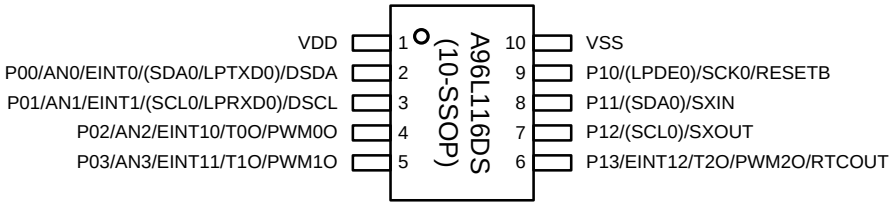



**NOTES:**

1. For the On-Chip Debugging, ISP assigns P0[1:0] pins for DSCL and DSDA respectively.
2. The P07 and P2[3:1] pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16-pin package is used.

### 3.1.4 A96L116DS (10-SSOP)

**Figure 37. A96L116DS 10-SSOP Pinouts**




**NOTES:**

1. For the On-Chip Debugging, ISP assigns P0[1:0] pins for DSCL and DSDA respectively.
2. The P0[7:4], P1[5:4], and P2[3:0] pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 10-pin package is used.

## 3.2 Pin Description

**Table 13. Pin Description**

| Pin Name | I/O | Function | @Reset | Shared with |
|---|---|---|---|---|
| P00 | I/O | The port 0 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. | Input | AN0/EINT0/(SDA0/LPTXD0)/DSDA |
| P01 | | | | AN1/EINT1/(SCL0/LPRXD0)/DSCL |
| P02 | | | | AN2/EINT10/T0O/PWM0O |
| P03 | | | | AN3/EINT11/T1O/PWM1O |
| P04 | | | | AN4/EC0 |
| P05 | | | | AN5/EC1/LPTXD0 |
| P06 | | | | AN6/LPRXD0 |
| P07 | | | | AN7/LPDE0 |
| P10 | I/O | Port 1 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. | Input | (LPDE0)/SCK0/RESETB |
| P11 | | | | (SDA0)/SXIN |
| P12 | | | | (SCL0)/SXOUT |
| P13 | | | | EINT12/T2O/PWM2O/RTCOUT |
| P14 | | | | EINT2/MOSI0/XOUT |
| P15 | | | | EINT3/MISO0/XIN |
| P20 | I/O | Port 2 is a bit-programmable I/O port which can be configured as a Schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. | Input | EC2/SS0 |
| P21 | | | | SDA/(MOSI0) |
| P22 | | | | SCL/(MISO0) |
| P23 | | | | (SCK0) |
| EINT0 | I/O | External interrupt inputs | Input | P00/AN0/(SDA0/LPTXD0)/DSDA |
| EINT1 | | | | P01/AN1/(SCL0/LPRXD0)/DSCL |
| EINT2 | | | | P14/MOSI0/XOUT |
| EINT3 | | | | P15/MISO0/XIN |
| EINT10 | I/O | External interrupt input and Timer 0 capture input | Input | P02/AN2/T0O/PWM0O |
| EINT11 | | External interrupt input and Timer 1 capture input | | P03/AN3/T1O/PWM1O |
| EINT12 | | External interrupt input and Timer 2 capture input | | P13/T2O/PWM2O |

**Table 13. Pin Description (continued)**

| Pin Name | I/O | Function | @reset | Shared with |
|---|---|---|---|---|
| T0O | I/O | Timer 0 interval output | Input | P02/AN2/EINT10/PWM0O |
| T1O | I/O | Timer 1 interval output | Input | P03/AN3/EINT11/PWM1O |
| T2O | I/O | Timer 2 interval output | Input | P13/EINT12/PWM2O |
| PWM0O | I/O | Timer 0 pulse output | Input | P02/AN2/EINT10/T0O |
| PWM1O | I/O | Timer 1 pulse output | Input | P03/AN3/EINT11/T1O |
| PWM2O | I/O | Timer 2 pulse output | Input | P13/EINT12/T2O |
| EC0 | I/O | Timer 0 event count input | Input | P04/AN4 |
| EC1 | I/O | Timer 1 event count input | Input | P05/AN5/LPTXD0 |
| EC2 | I/O | Timer 2 event count input | Input | P20/SS0 |
| AN0 | I/O | A/D converter analog input channels | Input | P00/EINT0/(SDA0/LPTXD0)/DSDA |
| AN1 | | | | P01/EINT1/(SCL0/LPRXD0)/DSCL |
| AN2 | | | | P02/EINT10/T0O/PWM0O |
| AN3 | | | | P03/EINT11/T1O/PWM1O |
| AN4 | | | | P04/EC0 |
| AN5 | | | | P05/EC1/LPTXD0 |
| AN6 | | | | P06/LPRXD0 |
| AN7 | | | | P07/LPDE0 |
| LPTXD0 | I/O | Low power UART data output | Input | P05/AN5/EC1<br>(P00/AN0/EINT0/(SDA0)/DSDA) |
| LPRXD0 | I/O | Low power UART data input | Input | P06/AN6<br>(P01/AN1/EINT1/(SCL0)/DSCL) |
| LPDE0 | I/O | Low power UART DE signal output | Input | P07/AN7<br>(P10/SCK0/RESETB) |
| MOSI0 | I/O | SPI master output, slave input | Input | P14/EINT2/XOUT<br>(P21/SDA0) |
| MISO0 | I/O | SPI master input, slave output | Input | P15/EINT3/XIN<br>(P22/SCL0) |
| SCK0 | I/O | SPI clock input/output | Input | P10/(LPDE0)/RESETB<br>(P23) |
| SS0 | I/O | SPI slave select input | Input | P20/EC2 |

**Table 13. Pin Description (continued)**

| Pin Name | I/O | Function | @reset | Shared with |
|---|---|---|---|---|
| SCL0 | I/O | I2C clock input/output | Input | P22/(MISO0)<br>(P01/AN1/EINT1/LPRXD0/DSCL)<br>(P12/SXOUT) |
| SDA0 | I/O | I2C data input/output | Input | P21/(MOSI0)<br>(P00/AN0/EINT0/LPTXD0/DSDA)<br>(P11/SXIN) |
| RTCOUT | I/O | Real time clock output | Input | P13/EINT12/T2O/PWM2O |
| RESETB | I/O | System reset pin with a pull-up resistor when it is selected as the RESETB by “CONFIGURE OPTION” | Input | P10/(LPDE0)/SCK0 |
| DSDA | I/O | On chip debugger data input/output | Input | P00/AN0/EINT0/(SDA0/LPTXD0) |
| DSCL | I/O | On chip debugger clock input | Input | P01/AN1/EINT1/(SCL0/LPRXD0) |
| XIN | I/O | Main oscillator pins | Input | P15/EINT3/MISO0 |
| XOUT | | | | P14/EINT2/MOSI0 |
| SXIN | I/O | Sub oscillator pins | Input | P11/(SDA0) |
| SXOUT | | | | P12/(SCL0) |
| VDD, VSS | – | Power input pins | – | – |

**NOTES:**

1. The P10/RESETB pin is configured as one of P10 and RESETB pin by the “CONFIGURE OPTION”.
2. The P15/XIN and P14/XOUT pins are configured as function pins by s/w control.
3. The P11/SXIN and P12/SXOUT pins are configured as a function pin by s/w control.
4. If the P00/DSDA and P01/DSCL pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
5. The P00/DSDA and P01/DSCL pins are configured as inputs with internal pull-up resistors only during the reset or power-on reset.

# 4. Electrical Characteristics

## 4.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to VSS.

### 4.1.1 Minimum and Maximum Values

Unless otherwise specified, our production tests guarantee the minimum and maximum values of the device under the worst-case conditions of ambient temperature, supply voltage, and frequency. These tests are performed on 100% of the devices with an ambient temperature of $T_A$ = 25°C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulations, and/or technical characteristics are not tested in production but are indicated in the table footnotes. The minimum and maximum values are obtained based on the characterization by referencing the sample test.

### 4.1.2 Typical Values

Unless otherwise specified, typical data are based on the conditions of TA = 25°C and VDD = 5.0 V. The typical data are provided only as design recommendations and are not tested. The typical accuracy values of the ADC are established by characterizing a batch of samples from a standard diffusion lot across the entire temperature range, with 95% of the devices having an error that is equal to or less than the indicated value.

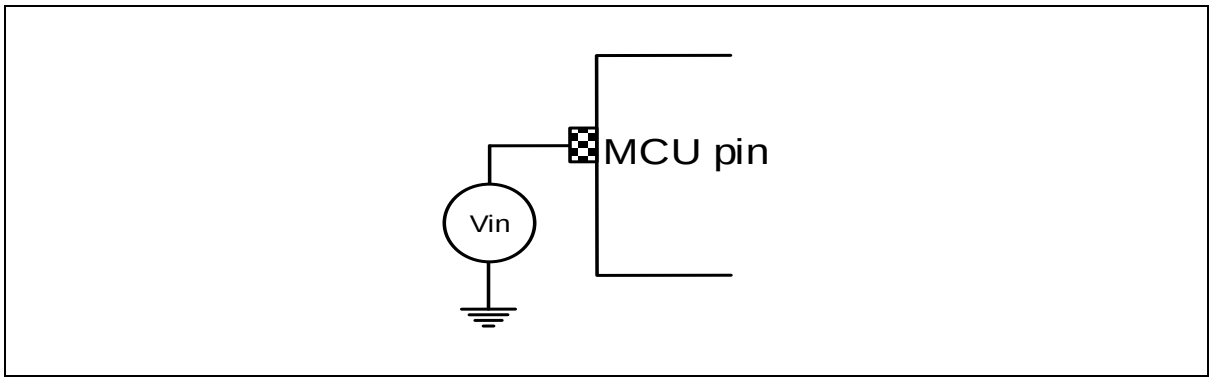
### 4.1.3 Typical Curves

Unless otherwise specified, all typical curves are provided only as design recommendations and are not tested.

### 4.1.4 Pin Input Voltage

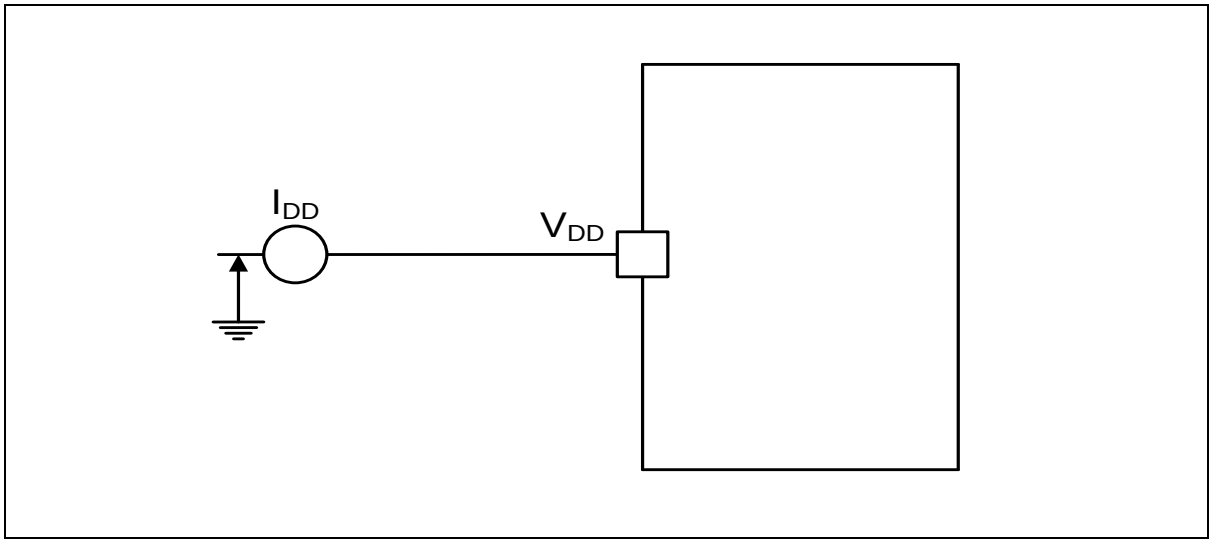
The input voltage measurement on a pin of the device is described in Figure 38.

**Figure 38. Pin Input Voltage**




### 4.1.5 Current Consumption Measurement

**Figure 39. Current Consumption Measurement**

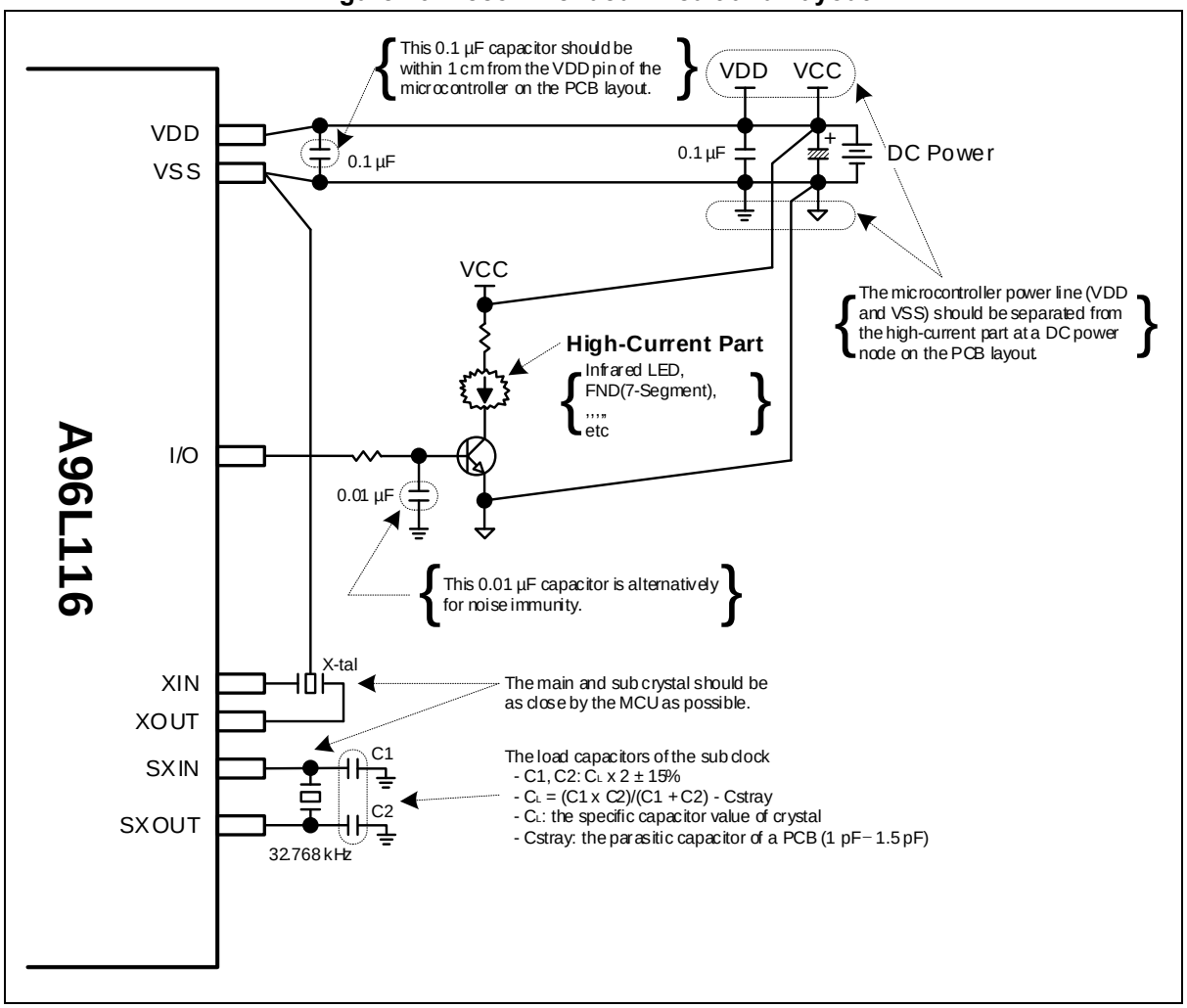


### 4.1.6 Power Supply Diagram

#### 4.1.6.1 Recommended Circuit and Layout

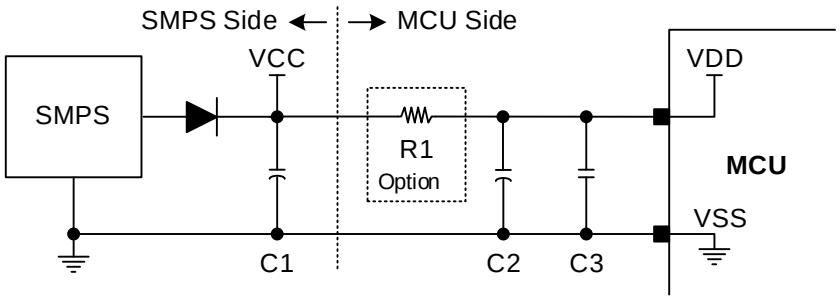
The Figure 40 is a recommended circuit and layout for A96L116.

**Figure 40. Recommended Circuit and Layout**



#### 4.1.6.2 Recommended Circuit and Layout with SMPS Power

**Figure 41. Recommended Circuit and Layout with SMPS Power**




1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   - Recommended C1: 470 µF/25 V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   - Recommended R1: 10 Ω – 20 Ω
   - Recommended C2: 47 µF/25 V more
   - The R1 and C2 should be as close by the C3 as possible.
   - The R1 is optional so it may not apply.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   - Recommended C3: ceramic capacitor 2.2 µF more
   - The C3 should be within 1 cm from VDD pin of the microcontroller on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of the microcontroller.

## 4.2 Absolute maximum ratings

Exceeding stresses specified in Table 14 for voltage characteristics, Table 14 for current characteristics, or Table 15 for thermal characteristics may result in permanent damage to the device. The values listed in the tables are stress ratings only and do not imply that the device will function correctly under these conditions. Prolonged exposure to these maximum rating conditions may impact the device's reliability. It is important to operate the device within its specified maximum ratings to ensure reliable performance.

**Table 14. Voltage Characteristics**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| VDD – VSS(1) | External main supply voltage (including VDD) | –0.3 | 4.0 | V |
| $V_I$ | Input voltage on I/O | –0.3 | Max. (VDD) + 0.3 | V |
| $V_O$ | Output voltage on I/O | –0.3 | Max. ($V_{DD}$) + 0.3 | V |

**NOTES:**

1. All main power ($V_{DD}$) and ground ($V_{SS}$) pins must always be connected to the external power supply, within the permitted range.
2. $V_I$ maximum must always be respected.

**Table 15. Absolute Maximum Ratings**

| Parameter | Symbol | Rating | Unit | Remark |
|---|---|---|---|---|
| Supply Voltage | VIN | –0.3 to +4.0 | V | – |
| Normal Voltage Pin | VI | –0.3 to VDD + 0.3 | V | Voltage on any pin with respect to VSS |
| | VO | –0.3 to VDD + 0.3 | V | |
| | IOH | –15 | mA | Maximum current output sourced by ($I_{OH}$ per I/O pin) |
| | ∑IOH | –60 | mA | Maximum current ($\sum I_{OH}$) |
| | IOL | 20 | mA | Maximum current sunk by ($I_{OL}$ per I/O pin) |
| | ∑IOL | 120 | mA | Maximum current ($\sum I_{OL}$) |
| Total Power Dissipation | PT | 600 | mW | – |
| Operating Temperature | TOP | –40 to +85 | °C | – |
| Storage Temperature | TSTG | –65 to +150 | °C | – |

**Caution:**

1. Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

**Table 16. Thermal Characteristics**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_{OP}$ | Operating temperature (commercial grade) | –40 to +85 | °C |
| $T_{STG}$ | Storage temperature range | –65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | °C |

## 4.3 Operating Conditions

### 4.3.1 Recommended Operating Conditions

**Table 17. Recommended Operating Conditions**

($T_A$ = –40°C to +85°C)

| Parameter | Symbol | Conditions | | | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Operating Voltage | VDD | fx = 32 to 38 kHz | SX-tal | | 1.71 | 3.6 | V |
| | | fx = 0.4 to 4.2 MHz | X-tal | Ceramic | 1.8 | 3.6 | |
| | | | | Crystal | 2.0 | 3.6 | |
| | | fx = 0.4 to 8 MHz | X-tal | | 2.4 | 3.6 | |
| | | fx = 0.4 to 12 MHz | | | 2.7 | 3.6 | |
| | | fx = 0.5 to 16 MHz | HFIRC | | 1.71 | 3.6 | |
| | | fx = 40 kHz | LFIRC | | 1.71 | 3.6 | |
| Operating Temperature | $T_{OPR}$ | VDD = 1.71 V to 3.6V | | | –40 | 85 | °C |

### 4.3.2 Operating Voltage Range

**Figure 42. Operating Voltage Range (Main OSC)**

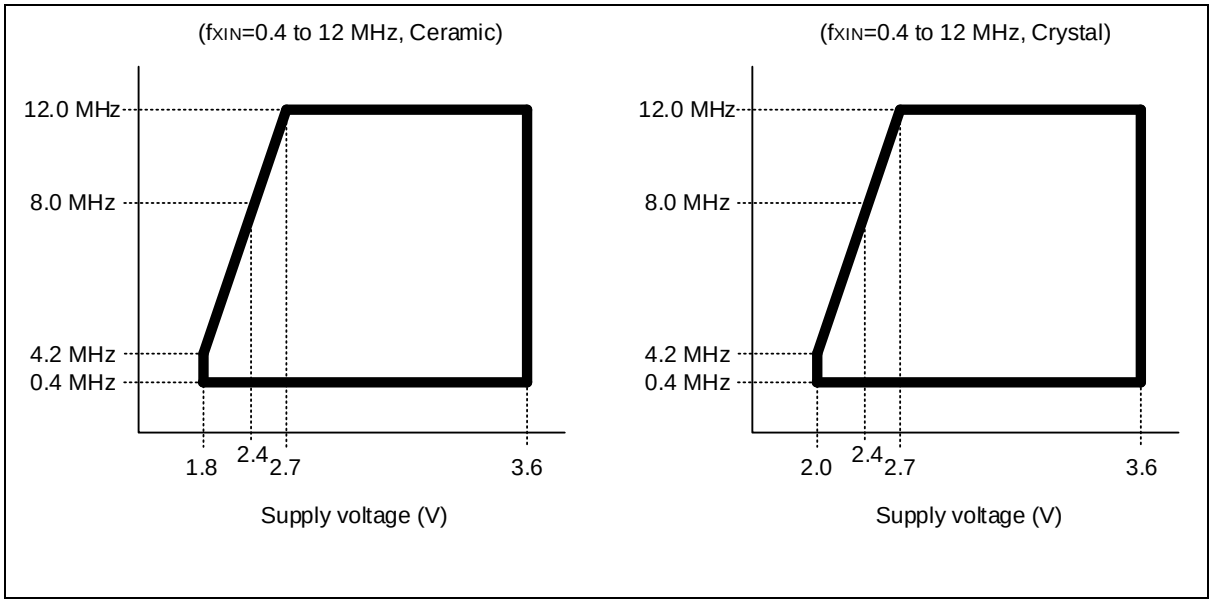
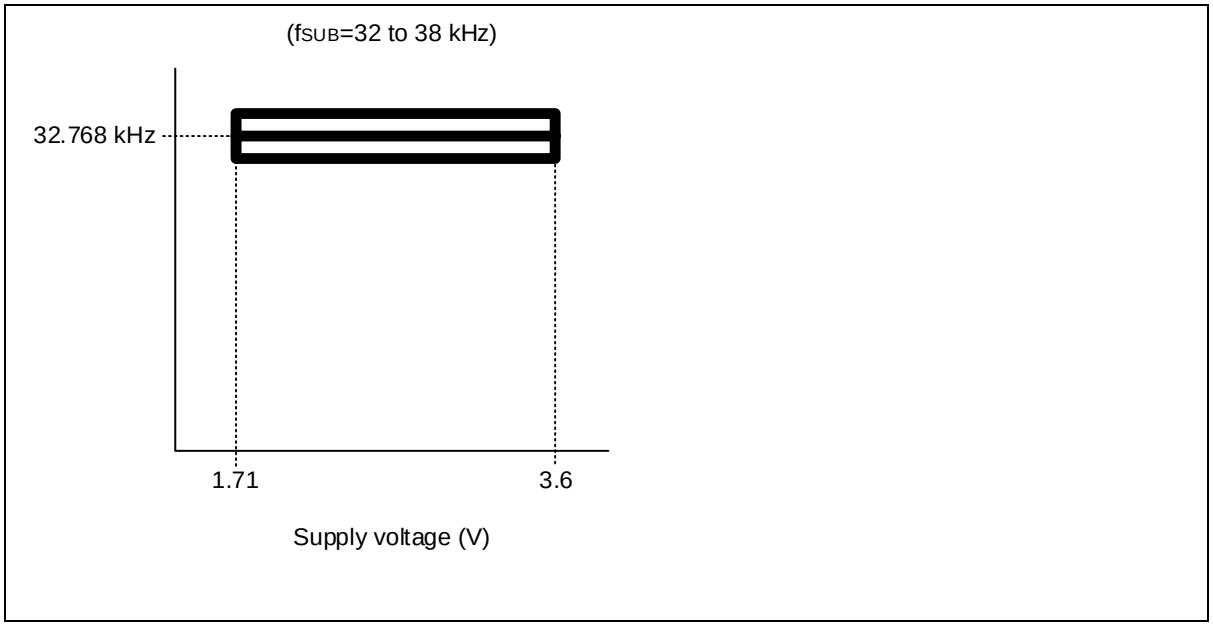



**Figure 43. Operating Voltage Range (Sub OSC)**



### 4.3.3 Typical Characteristics

Figures and tables described in this chapter can be used only for design guidance and are not tested or guaranteed. In graphs or tables some data may exceed the specified operating range and can be only for information. The device is guaranteed to operate properly only within the specified range.

The data presented in this chapter is a statistical summary of data collected on units from different lots over a period. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively where σ is standard deviation.

**Figure 44. Main RUN (IDD1) Current**

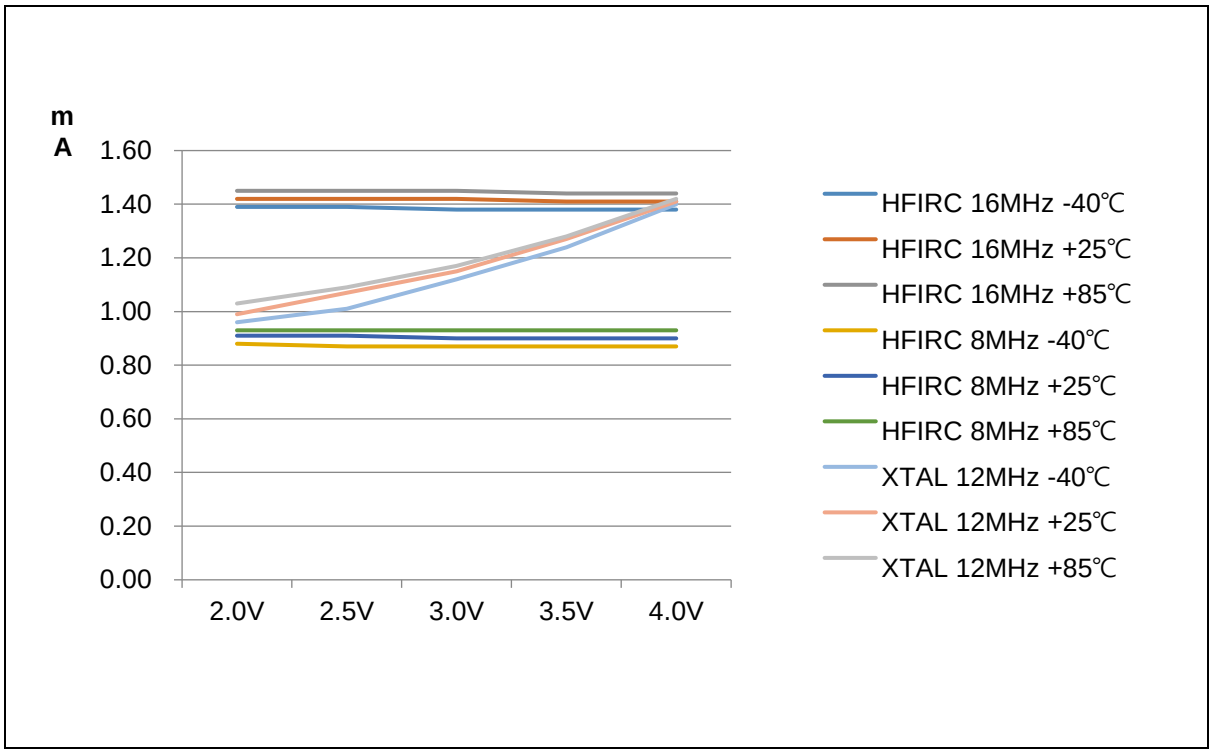


**Figure 45. Main IDLE (IDD2) Current**

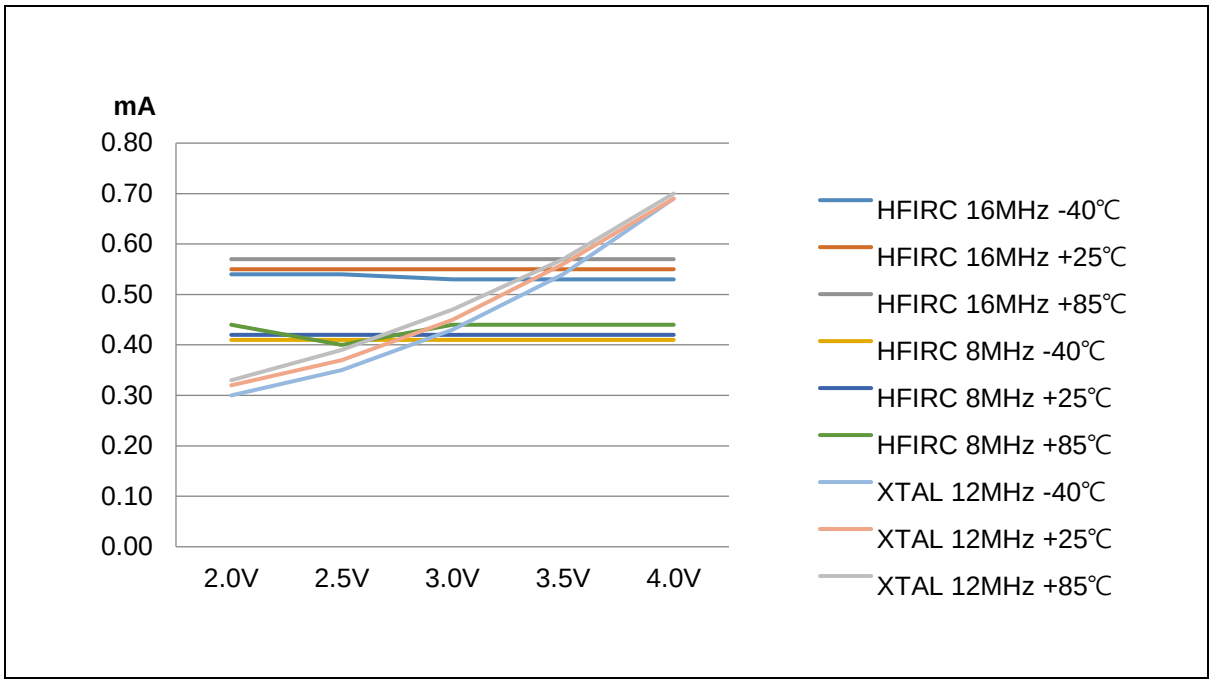



**Figure 46. Sub RUN (IDD3) Current**

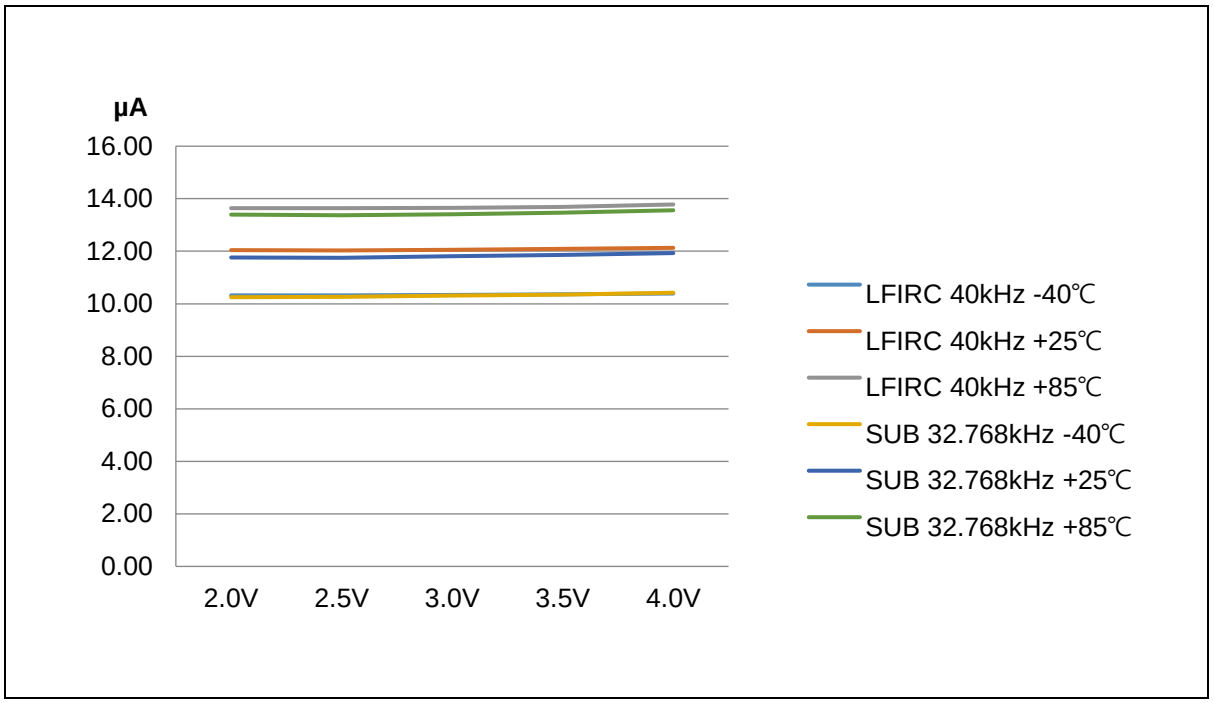


**Figure 47. Sub IDLE (IDD4) Current**

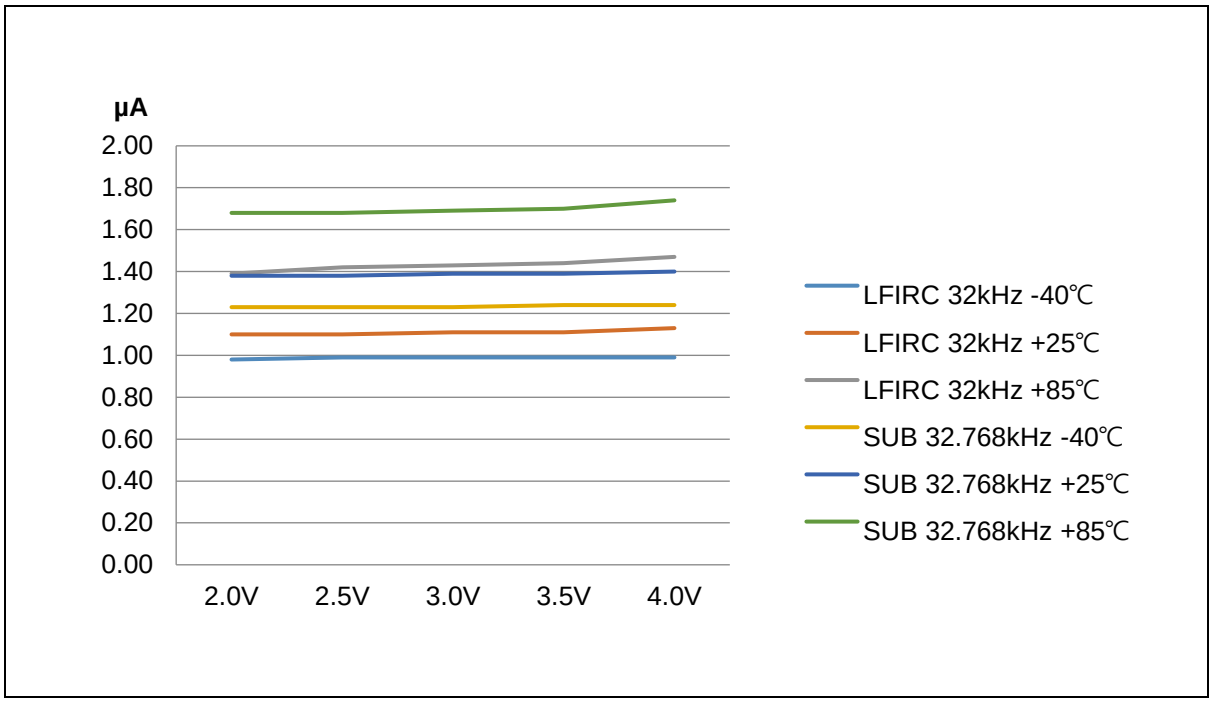
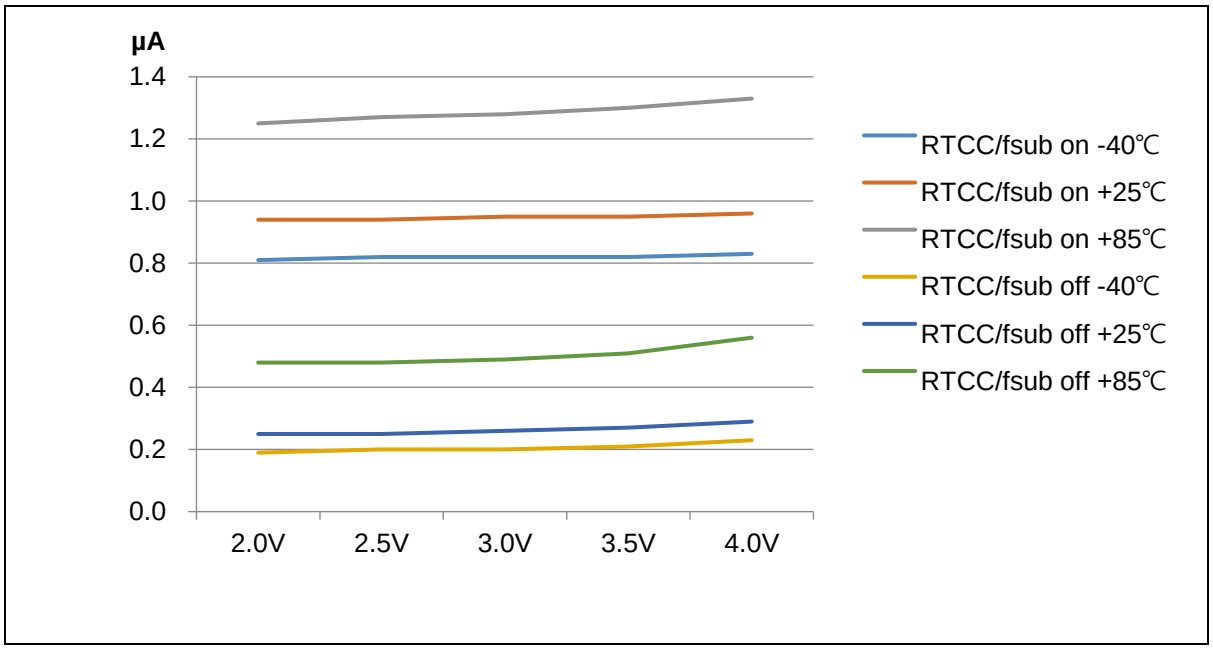



**Figure 48. STOP (IDD5, RTCC/$f_{SUB}$ On/Off) Current**



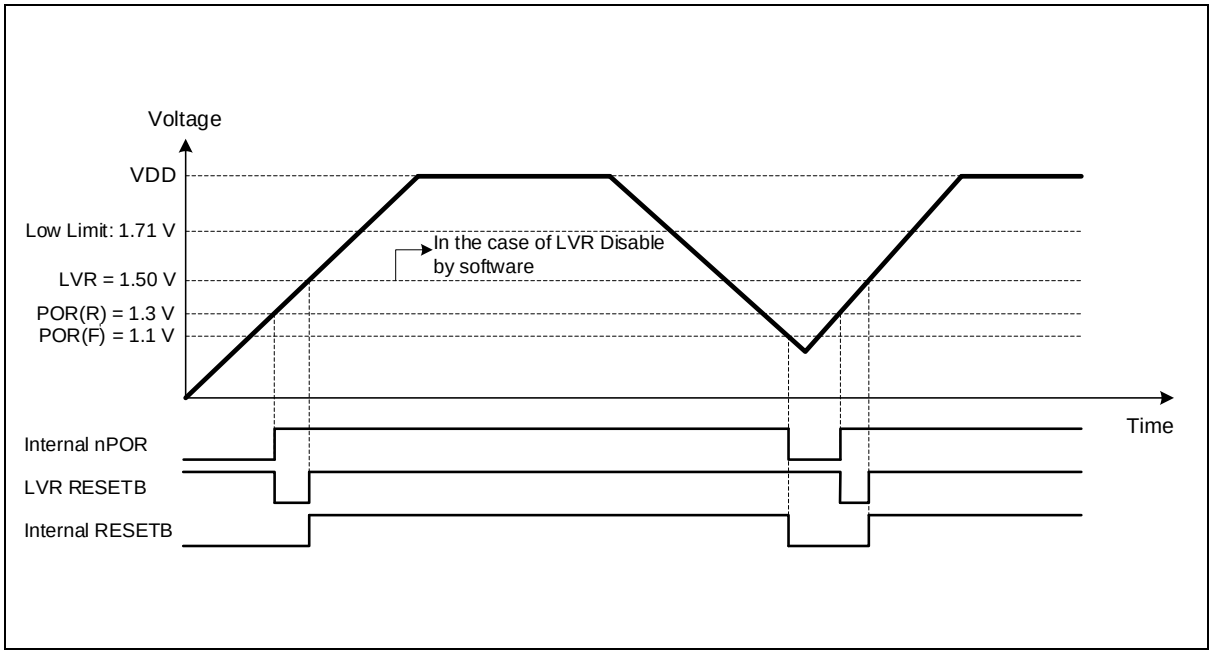
### 4.3.4 Power-On Reset Characteristics

**Table 18. Power-On Reset Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RESET release level | $V_{POR}$ | – | – | 1.2 | – | V |
| Hysteresis | △V | – | – | 0.1 | – | V |
| VDD Voltage Rising Time | $t_R$ | 0.2V – 2V | 0.05 | – | 100 | V/ms |
| POR current | $I_{POR}$ | – | – | 50 | 100 | nA |

**Figure 49. Power-On Reset Timing**



### 4.3.5 Low-Voltage Reset and Indicator Characteristics (LVR and LVI)

**Table 19. LVR and LVI Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VLVR<br>VLVI | Detection level | LVR: All levels<br>LVI: other levels except 1.50 V<br>1.50 V level: Rising edge voltage<br>Other levels: Falling edge voltage | | – | 1.50 | 1.70 | V |
| | | | | 1.72 | 1.87 | 2.02 | |
| | | | | 1.87 | 2.02 | 2.17 | |
| | | | | 2.02 | 2.17 | 2.32 | |
| | | | | 2.17 | 2.32 | 2.47 | |
| | | | | 2.27 | 2.47 | 2.67 | |
| | | | | 2.44 | 2.64 | 2.84 | |
| | | | | 2.58 | 2.78 | 2.98 | |
| △V | Hysteresis | – | | – | 40 | 150 | mV |
| $t_{LW}$ | Minimum pulse width | – | | 100 | – | – | µs |
| $I_{BL}$ | LVR and LVI current | Enable, One of two | VDD = 3 V | – | 200 | 400 | nA |
| | | Enable, Both | | – | 250 | 500 | |
| | | Disable | | – | – | 10 | |

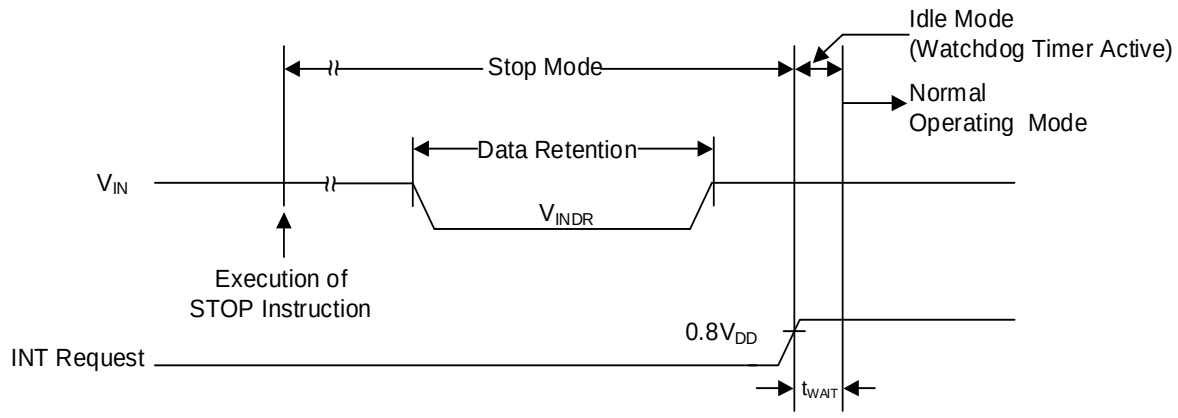
### 4.3.6 Data Retention voltage in STOP mode

**Table 20. Data Retention Voltage in STOP Mode**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDDR}$ | Data retention supply voltage | — | 1.71 | — | 3.6 | V |
| $I_{DDDR}$ | Data retention supply current | VDDDR = 1.71 V ($T_A$= 25°C), STOP mode | — | — | 1 | µA |

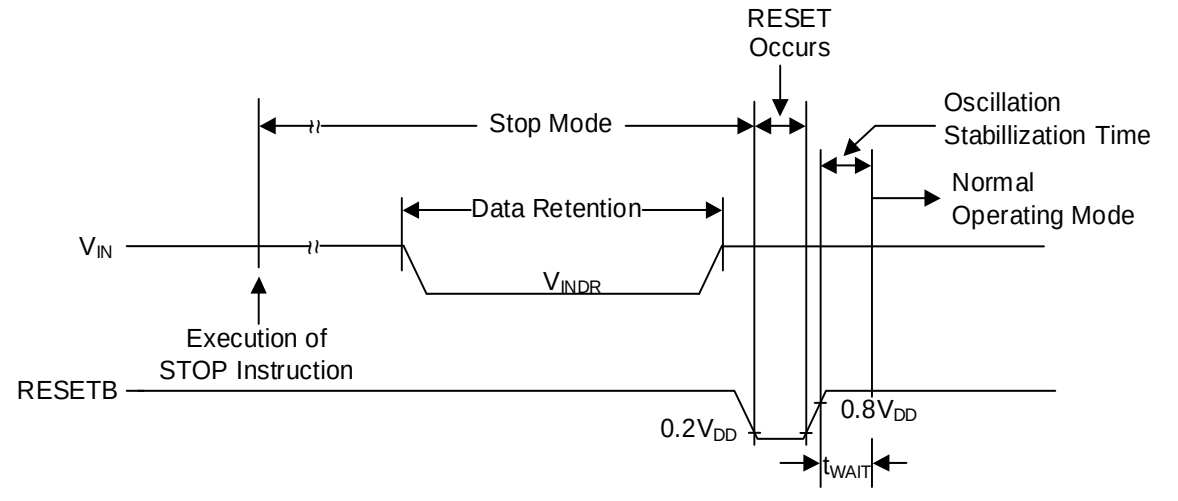
**Figure 50. STOP Mode Release Timing when Initiated by an Interrupt**




**NOTE:**

1. tWAIT is the same as (the selected bit overflow of BIT) x 1/ (BIT clock)

**Figure 51. STOP Mode Release Timing when Initiated by RESETB**




**NOTE:**

1. tWAIT is the same as (4096 x 4 x 16/$f_{HFIRC}$) = (16.4 ms at fx=1 MHz)

### 4.3.7 Flash Memory Characteristics

#### 4.3.7.1 Internal Flash Characteristics

**Table 21. Internal Flash Characteristics**

($T_A$= +25°C, VDD=1.71 V to 3.6 V)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Sector write time | $t_{FSW}$ | — | — | 3.0 | 3.5 | ms |
| Sector erase time | $t_{FSE}$ | — | — | 3.0 | 3.5 | |
| Code write protection time | $t_{FHL}$ | — | — | 3.0 | 3.5 | |
| Page buffer reset time | $t_{FBR}$ | — | — | — | 5 | µs |
| Flash program Voltage | $V_{PGM}$ | On erase/write | 2.0 | — | 3.6 | V |
| System clock frequency | $f_{SCLK}$ | — | 0.4 | — | — | MHz |
| Endurance of write/erase | $N_{FWE}$ | Sector erase/write | 10,000 | — | — | cycles |
| Flash Retention Time | $t_{FRT}$ | — | 10 | — | — | years |

#### 4.3.7.2 Internal Data Flash characteristics

**Table 22. Internal Data Flash Characteristics**

($T_A$= +25°C, VDD=1.71 V to 3.6 V)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Sector write time | $t_{DFSW}$ | — | — | 3.0 | 3.5 | ms |
| Sector erase time | $t_{DFSE}$ | — | — | 3.0 | 3.5 | |
| Page buffer reset time | $t_{DFBR}$ | — | — | — | 5 | µs |
| Data Flash program voltage | $V_{DPGM}$ | On erase/write | 2.0 | — | 3.6 | V |
| System clock frequency | $f_{SCLK}$ | — | 0.4 | — | — | MHz |
| Endurance of write/erase | $N_{DFWE}$ | Sector erase/write | 100,000 | — | — | cycles |
| Flash Retention Time | $t_{DFRT}$ | — | 10 | — | — | years |

### 4.3.8 Current Consumption Characteristics

The amount of current consumed by the device is determined by various factors and parameters, including but not limited to the operating voltage, ambient temperature, load on I/O pins, software configuration, operating frequency, switching rate of I/O pins, location of the program in memory, and the binary code being executed.

The current consumption is measured under the conditions specified in Table 23.

**Table 23. Supply Current Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD1}$ (RUN) | Supply current | $f_{HFIRC}$ = 16 MHz, VDD = 3 V | | — | 1.5 | 2.2 | mA |
| | | $f_{HFIRC}$ = 8 MHz, VDD = 3 V | | — | 0.8 | 1.2 | |
| | | fxin = 12 MHz, VDD = 3 V | | — | 1.3 | 2.0 | |
| $I_{DD2}$ (IDLE) | | $f_{HFIRC}$ = 16 MHz, VDD = 3 V | | — | 0.6 | 0.9 | mA |
| | | $f_{HFIRC}$ = 8 MHz, VDD = 3 V | | — | 0.4 | 0.6 | |
| | | fxin = 12 MHz, VDD = 3 V | | — | 0.6 | 0.9 | |
| $I_{DD3}$ (RUN) | | $f_{SUB}$ = 32.768 kHz ($C_L$: 7 pF), or $f_{LFIRC}$ = 40 kHz, VDD = 3 V | $T_A$= 25°C | — | 12.0 | 19.0 | µA |
| | | | $T_A$= 85°C | — | 14.0 | 22.0 | |
| $I_{DD4}$ (IDLE) | | $f_{SUB}$ = 32.768 kHz ($C_L$: 7 pF), or $f_{LFIRC}$ = 40 kHz, VDD = 3 V | $T_A$= 25°C | — | 1.8 | 3.6 | µA |
| | | | $T_A$= 85°C | — | 2.1 | 7.9 | |
| $I_{DD5}$ (STOP) | | VDD = 3 V, RTCC/ $f_{SUB}$ Off | $T_A$= 25°C | — | 0.35 | 0.9 | µA |
| | | | $T_A$= 85°C | — | 1.5 | 5.0 | |
| | | VDD = 3 V, RTCC/ $f_{SUB}$ On, $T_A$= 25°C | | — | 0.9 | 1.6 | µA |

**NOTES:**

1. Where the fxin is an external main oscillator, the fsub is an external sub oscillator (SUBISET = 0x5), the HFIRC is an internal high frequency RC oscillator, the LFIRC is an internal low frequency RC oscillator and the fx is the selected system clock.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

#### 4.3.8.1 I/O System Current Consumption

In the I/O system, current consumption can be separated into two components: Static and Dynamic.

#### 4.3.8.2 I/O Static Current Consumption

When I/O pins configured as inputs with pull-up are externally held low, they generate a current consumption. This current consumption can be simply calculated using the values of the pull-up/pull-down resistors specified in the I/O port characteristics.

To estimate the current consumption for output pins, any external pull-down or load must also be taken into consideration.

The current consumption of I/O pins configured as inputs may increase when an intermediate voltage level is applied externally. Therefore, it is recommended to avoid applying an intermediate voltage level if there is no specific need for this configuration.

#### 4.3.8.3 I/O Dynamic Current Consumption

Besides the internal peripheral current consumption, the application's I/Os also contribute to the overall current consumption. When an I/O pin switches, it draws current from the microcontroller's supply voltage to power the I/O pin circuitry and to charge/discharge any capacitive loads (either internal or external) connected to the pin.

### 4.3.9 External Clock Source Characteristics

#### 4.3.9.1 External Main Oscillator

The external main oscillator (XMOSC) clock can be generated using a crystal/ceramic resonator oscillator with a frequency range of 0.4 to 12 MHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 24.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

**Table 24. Main Oscillator Characteristics**

($T_A$= –40°C to +85°C, VDD=1.8 V to 3.6 V)

| Oscillator | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Crystal | Main oscillation frequency | 2.0 V to 3.6 V | 0.4 | — | 4.2 | MHz |
| | | 2.4 V to 3.6 V | 0.4 | — | 8.0 | |
| | | 2.7 V to 3.6 V | 0.4 | — | 12.0 | |
| Ceramic Oscillator | Main oscillation frequency | 1.8 V to 3.6 V | 0.4 | — | 4.2 | |
| | | 2.4 V to 3.6 V | 0.4 | — | 8.0 | |
| | | 2.7 V to 3.6 V | 0.4 | — | 12.0 | |
| External Clock | XIN input frequency | 1.8 V to 3.6 V | 0.4 | — | 4.2 | |
| | | 2.4 V to 3.6 V | 0.4 | — | 8.0 | |
| | | 2.7 V to 3.6 V | 0.4 | — | 12.0 | |

**Figure 52. Crystal/Ceramic Oscillator**

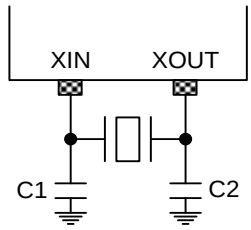
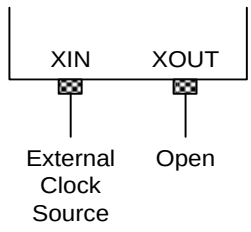



**Figure 53. External Clock**

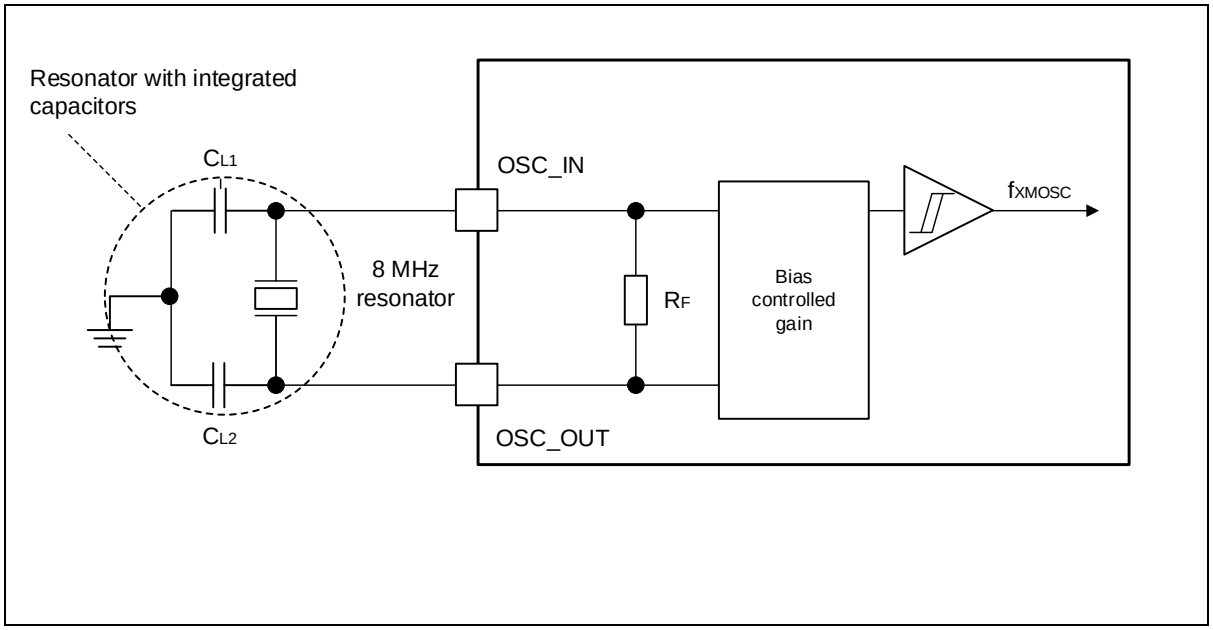


It is recommended to use high-quality external ceramic capacitors designed for high-frequency applications and selected to match the requirements of the crystal or resonator. The CL1 and CL2 capacitors are usually of the same size, and the crystal manufacturer typically specifies a load capacitance that is the series combination of both capacitors. The capacitance values of the CL1 and CL2 capacitors should be set by considering the parasitic capacitance of the printed circuit board (PCB) and microcontroller pins, which is approximately twice the specified load capacitance of the crystal.

A rough estimate of the combined pin and board capacitance is typically in the range of 2 to 4 pF, which can serve as a guideline for appropriately sizing the CL1 and CL2 capacitors.

Figure 54 shows a circuit diagram of a typical application with an 8 MHz crystal.

**Figure 54. Typical Application with an 8 MHz Crystal**



#### 4.3.9.2 External Sub-Oscillator

The external sub-oscillator (XSOSC) clock can be generated using a crystal/ceramic resonator oscillator with 32.768 kHz. The information provided in this paragraph is based on characterization results obtained using typical external components listed in Table 25.

To minimize output distortion and startup stabilization time, it is recommended to place the resonator and load capacitors as close as possible to the oscillator pins in the application.

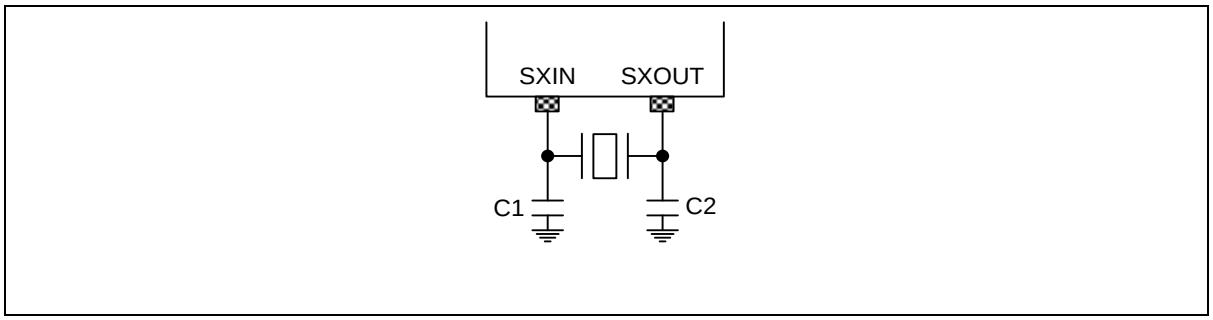
For further information on the resonator characteristics such as frequency, package, and accuracy, it is advisable to refer to the crystal resonator manufacturer.

**Table 25. External Sub-Oscillator Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V)

| Oscillator | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Crystal | Sub oscillation frequency | 1.71 V to 3.6 V | 32 | 32.768 | 38 | kHz |

**Figure 55. Crystal Oscillator**



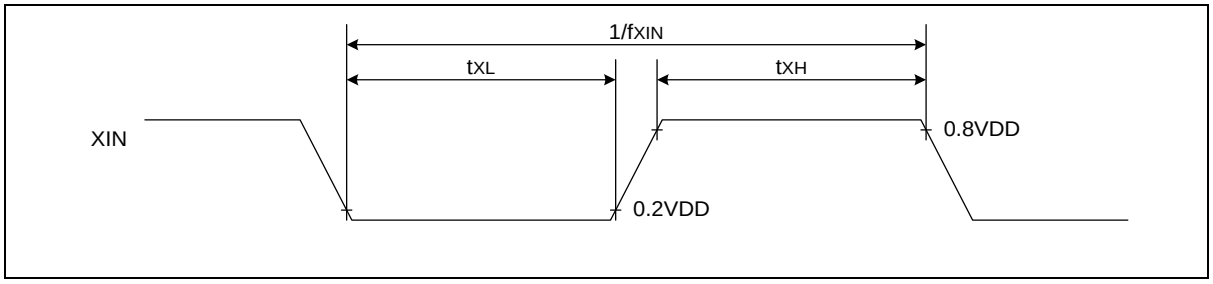
#### 4.3.9.3 Main Oscillator Stabilization Characteristics

**Table 26. Main Oscillator Stabilization Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V)

| Oscillator | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Crystal | fXIN ≥ 1 MHz, VDD = 2.0~3.6 V<br>Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range. | — | — | 60 | ms |
| Ceramic | fXIN ≥ 1 MHz, VDD = 1.8~3.6 V<br>Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range. | — | — | 10 | |
| External Clock | fXIN = 0.4 to 12 MHz<br>XIN input high and low width (tXL, tXH) | 42 | — | 1,250 | ns |

**Figure 56. Clock Timing Measurement at XIN**



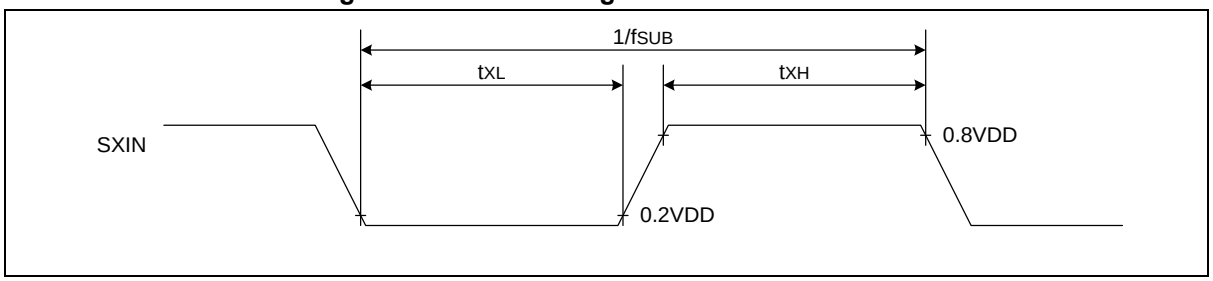

#### 4.3.9.4 Sub Oscillator Stabilization Characteristics

**Table 27. Sub Oscillator Stabilization Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V)

| Oscillator | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Crystal | — | — | — | 10 | sec |
| | VDD = 3 V, $T_A$= 25°C | — | 0.7 | 1.5 | |
| External Clock | SXIN input high and low width (tXL, tXH) | 5 | — | 15 | µs |

**Figure 57. Clock Timing Measurement at SXIN**



### 4.3.10 Internal Clock Source Characteristics

#### 4.3.10.1 High Frequency Internal RC Oscillator Characteristics

**Table 28. High Frequency Internal RC Oscillator Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HFIRC}$ | Frequency | — | — | 16 | — | MHz |
| | Tolerance | $T_A$ = 0 to +50°C | — | — | ±1.5 | % |
| | | $T_A$ = –40 to +85°C | | | ±2.0 | |
| $T_{OD}$ | Clock duty ratio | — | 40 | 50 | 60 | % |
| $t_{HFS}$ | Stabilization time | — | — | — | 2 | µs |
| $I_{HFIRC}$ | HFIRC Current | Enable | — | 200 | 350 | µA |
| | | Disable | — | — | 10 | nA |

#### 4.3.10.2 Low Frequency Internal RC Oscillator Characteristics

**Table 29. Low Frequency Internal RC Oscillator Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $f_{LFIRC}$ | Frequency | — | | 34 | 40 | 46 | kHz |
| $t_{LFS}$ | Stabilization time | — | | — | — | 100 | µs |
| $I_{LFIRC}$ | WDTRC current | Enable | VDD = 3.0 V | — | 450 | 650 | nA |
| | | Disable | | — | — | 10 | |

#### 4.3.10.3 Internal WatchDog Timer RC Oscillator Characteristics

**Table 30. Internal WDTRC Oscillator Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{WDTRC}$ | Frequency | — | 4.25 | 5 | 5.75 | kHz |
| $t_{WDTS}$ | Stabilization time | — | — | — | 1 | ms |
| $I_{WDTRC}$ | WDTRC current | Enable | — | 450 | 650 | nA |
| | | Disable | — | — | 10 | |

### 4.3.11 DC Characteristics

The parameters listed in Table 31 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 17.

**Table 31. I/O Port Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | All input pins, RESETB | 0.8×VDD | — | VDD | V |
| Input low voltage | $V_{IL}$ | All input pins, RESETB | — | — | 0.2×VDD | V |
| Output high voltage | $V_{OH}$ | All output ports, VDD = 3 V, IOH = –2 mA | VDD–1.0 | — | — | V |
| Output low voltage | $V_{OL}$ | All output ports, VDD = 3 V, IOL = 10 mA | — | — | 1.0 | V |
| Input high leakage current | $I_{IH}$ | All output ports | — | — | 1.0 | µA |
| Input low leakage current | $I_{IL}$ | All output ports | –1.0 | — | — | µA |
| Pull-up resistor | $R_{PU1}$ | VI=0 V, $T_A$=25°C, VDD = 3 V, All Input ports | 25 | 50 | 100 | kΩ |
| | $R_{PU2}$ | VI=0 V, $T_A$=25°C, VDD = 3 V, RESETB | 150 | 250 | 400 | kΩ |
| OSC feedback resistor | $R_{X1}$ | XIN = VDD, XOUT = VSS $T_A$=25°C, VDD = 3 V | 600 | 1,200 | 2,000 | kΩ |
| | $R_{X2}$ | $T_A$=25°C, VDD = 3 V | 4 | 7 | 14 | MΩ |

#### 4.3.11.1 Output Driving Current

The GPIOs can sink or source currents within the range specified by IOL and IOH.

To ensure compliance with the absolute maximum ratings specified in chapter 4.2, it is necessary to limit the number of I/O pins driving current in the user application.

- The total current sourced by all I/O pins on VDD and the maximum operating current of the microcontroller on VDD (during RUN mode) must not exceed the absolute maximum rating ΣIVDD specified in Table 15.
- The total current sunk by all I/O pins on GND and the maximum operating current of the microcontroller on GND (during Run mode) must not exceed the absolute maximum rating ΣIVSS specified in Table 15.

#### 4.3.11.2 Output Voltage Characteristics

Unless otherwise specified, the parameters in Table 32 are obtained through tests conducted under ambient temperature and supply voltage conditions, which are specified in Table 17.

**Table 32. Output Voltage Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output high level voltage for an I/O pin | VDD = 3 V, $I_{OH}$ = –2 mA | $V_{DD}$ – 1.0 | – | – | V |
| $V_{OL}$ | Output low level voltage for an I/O pin | VDD = 3 V, $I_{OL}$ = 10 mA | – | – | 1.0 | V |

#### 4.3.11.3 Input / Output Capacitance Characteristics

**Table 33. I/O Capacitance Characteristics**

($T_A$= –40°C to +85°C, VDD=0 V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | fx=1 MHz<br>Unmeasured pins are connected to VSS. | — | — | 10 | pF |
| $C_{OUT}$ | Output capacitance | | | | | |
| $C_{IO}$ | I/O capacitance | | | | | |

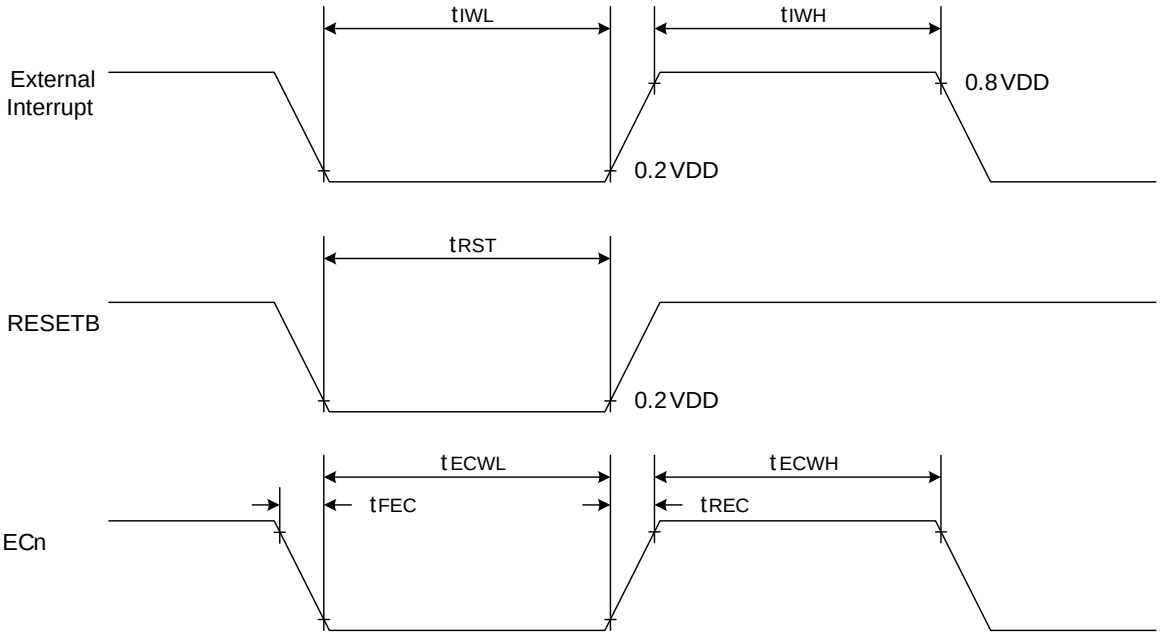
### 4.3.12 AC Characteristics

**Table 34. AC Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{RST}$ | RESETB input low width | VDD = 3 V | 10 | — | — | µs |
| $t_{IWH}$, $t_{IWL}$ | Interrupt input high, low width | All interrupt, VDD = 3 V | 200 | — | — | ns |
| $t_{ECWH}$, $t_{ECWL}$ | External counter input high, low pulse width | ECn, VDD = 3 V, Where n=0, 1, and 2 | 200 | — | — | |
| $t_{REC}$, $t_{FEC}$ | External counter transition time | ECn, VDD = 3 V, Where n=0, 1, and 2 | 20 | — | — | |
| $t_{WU0}$ | Wake-up from idle/stop mode | From HFIRC | — | 5 | 8 | µs |
| $t_{WU1}$ | | From LFIRC | — | — | 1,000 | |

**Figure 58. AC Timing**




**NOTE:**

1. n =0, 1 and 2.

### 4.3.13 ADC Characteristics

**Table 35. ADC Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, VSS=0 V)

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| — | Resolution | — | | — | 12 | — | bit |
| INL | Integral Non-linear | VDD = 2.4 V to 3.6 V, $f_x$=8 MHz | | — | — | ±5 | LSB |
| DNL | Differential Non-linearity | | | — | — | ±1 | |
| TOE | Top offset error | | | — | — | ±5 | |
| ZOE | Zero offset error | | | — | — | ±5 | |
| $t_{CON}$ | Conversion time | VDD = 2.7 V to 3.6 V | | 9 | — | — | us |
| | | VDD = 2.4 V to 3.6 V | | 12 | — | — | |
| | | VDD = 2.0 V to 3.6 V | | 28 | — | — | |
| $V_{AN}$ | Analog input voltage | — | | VSS | — | VDD | V |
| $V_{BGR}$ | Band gap reference voltage | $T_A$ = 25°C | | 890 | 940 | 990 | mV |
| IAN | A/DC input leakage current | VDD = 3 V | | — | — | 2 | µA |
| $I_{ADC}$ | ADC current | Enable | VDD = 3 V | — | 400 | 800 | µA |
| | | Disable | | — | — | 10 | nA |

**NOTES:**

1. Zero offset error is the difference between 0000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 1111111111 and the converted output for top input voltage (VDD).

### 4.3.14 Communication Interface Characteristics

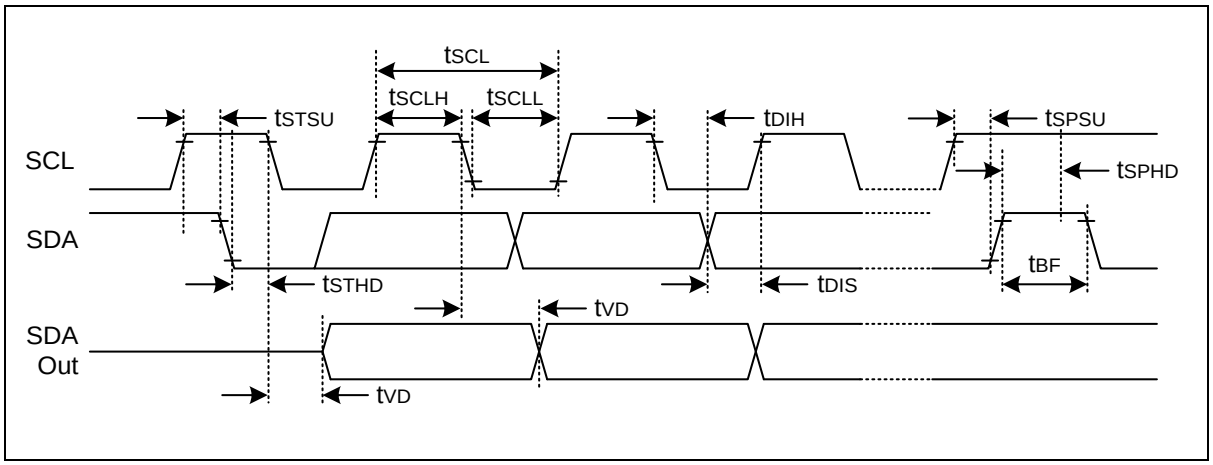
#### 4.3.14.1 I2C Characteristics

**Table 36. I2C Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V)

| Symbol | Parameter | Standard Mode | | High-Speed Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| tSCL | Clock frequency | 0 | 100 | 0 | 400 | kHz |
| tSCLH | Clock High Pulse Width | 4.0 | — | 0.6 | — | us |
| tSCLL | Clock Low Pulse Width | 4.7 | — | 1.3 | — | |
| tBF | Bus Free Time | 4.7 | — | 1.3 | — | |
| tSTSU | Start Condition Setup Time | 4.7 | — | 0.6 | — | |
| tSTHD | Start Condition Hold Time | 4.0 | — | 0.6 | — | |
| tSPSU | Stop Condition Setup Time | 4.0 | — | 0.6 | — | |
| tSPHD | Stop Condition Hold Time | 4.0 | — | 0.6 | — | |
| tVD | Output Valid from Clock | 0 | — | 0 | — | |
| tDIH | Data Input Hold Time | 0 | — | 0 | 1.0 | |
| tDIS | Data Input Setup Time | 250 | — | 100 | — | ns |

**Figure 59. I2C Timing**



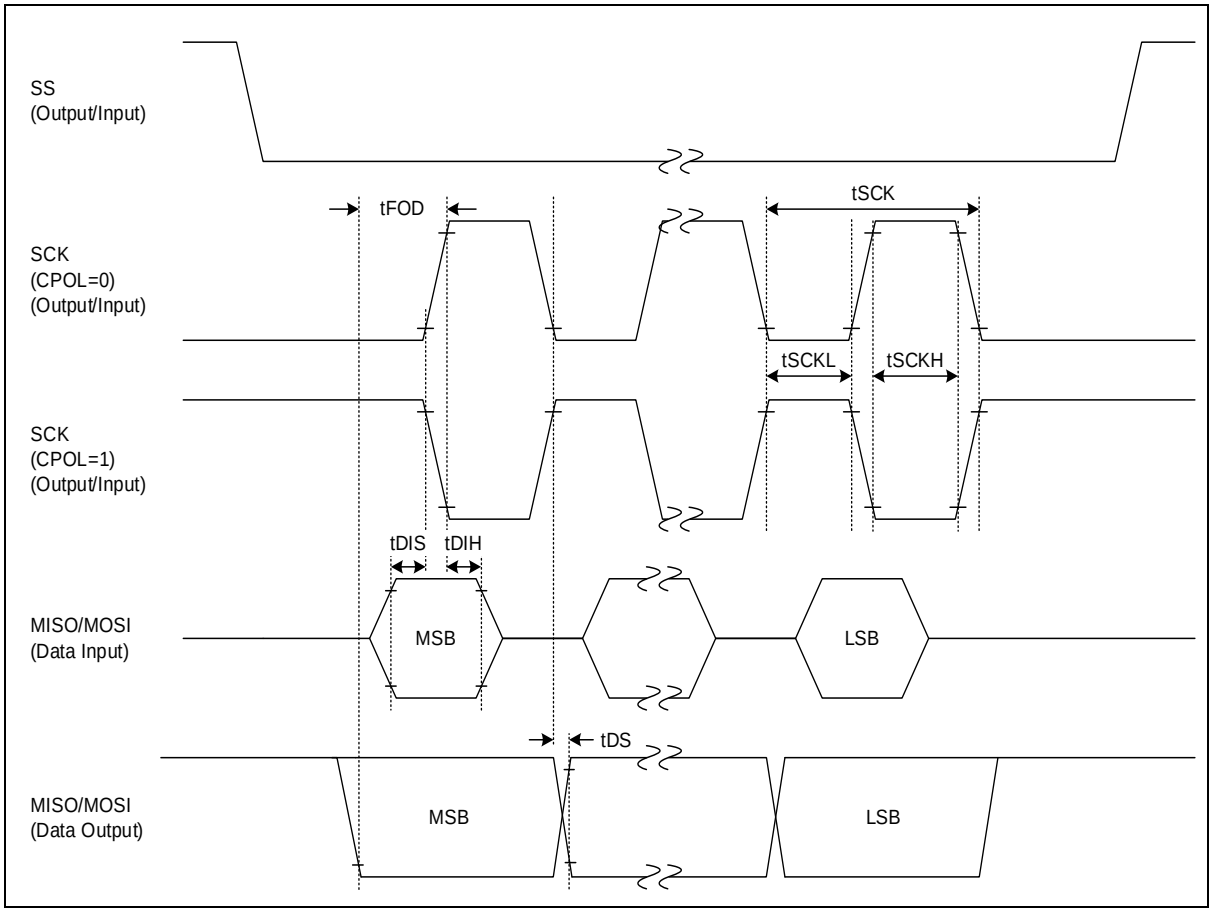
### 4.3.14.2 SPI Characteristics

**Table 37. SPI Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{SCK}$ | Output clock pulse period | Internal SCK source | 1,000 | — | — | ns |
| | Input clock pulse period | External SCK source | 1,000 | — | — | |
| $t_{SCKH}$ $t_{SCKL}$ | Output clock high, low pulse width | Internal SCK source | 400 | — | — | |
| | Input clock high, low pulse width | External SCK source | 400 | — | — | |
| $t_{FOD}$ | First output clock delay time | Internal/external SCK source | 500 | — | — | |
| $t_{DS}$ | Output clock delay time | — | — | — | 125 | |
| $t_{DIS}$ | Input setup time | — | 500 | — | — | |
| $t_{DIH}$ | Input hold time | — | 500 | — | — | |

**Figure 60. SPI Timing**



### 4.3.14.3 UART Timing Characteristics

**Table 38. UART Timing Characteristics**

($T_A$= –40°C to +85°C, VDD=1.71 V to 3.6 V, fx=11.1 MHz)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{SCK}$ | Serial port clock cycle time | 1,250 | $t_{CPU}$ × 16 | 1,650 | ns |
| $t_{S1}$ | Output data setup to clock rising edge | 590 | $t_{CPU}$ × 13 | — | |
| $t_{S2}$ | Clock rising edge to input data valid | — | — | 590 | |
| $t_{H1}$ | Output data hold after clock rising edge | $t_{CPU}$ – 50 | $t_{CPU}$ | — | |
| $t_{H2}$ | Input data hold after clock rising edge | 0 | — | — | |
| $t_{HIGH}$, $t_{LOW}$ | Serial port clock High, Low level width | 470 | $t_{CPU}$ × 8 | 970 | |

**Figure 61. UART Timing Characteristics**

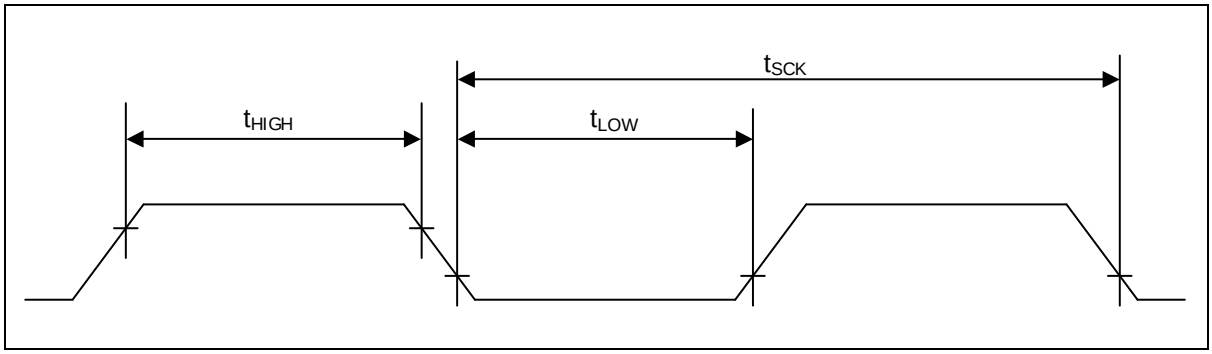
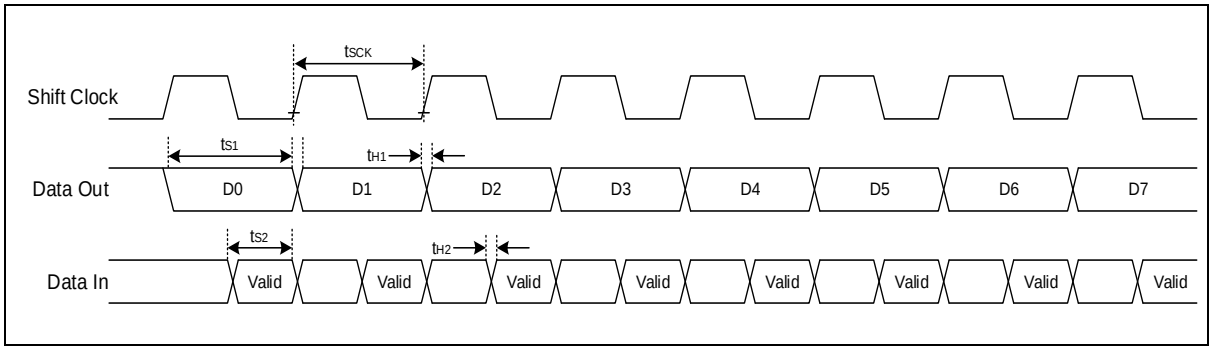



**Figure 62. Timing Waveform of UART Module**

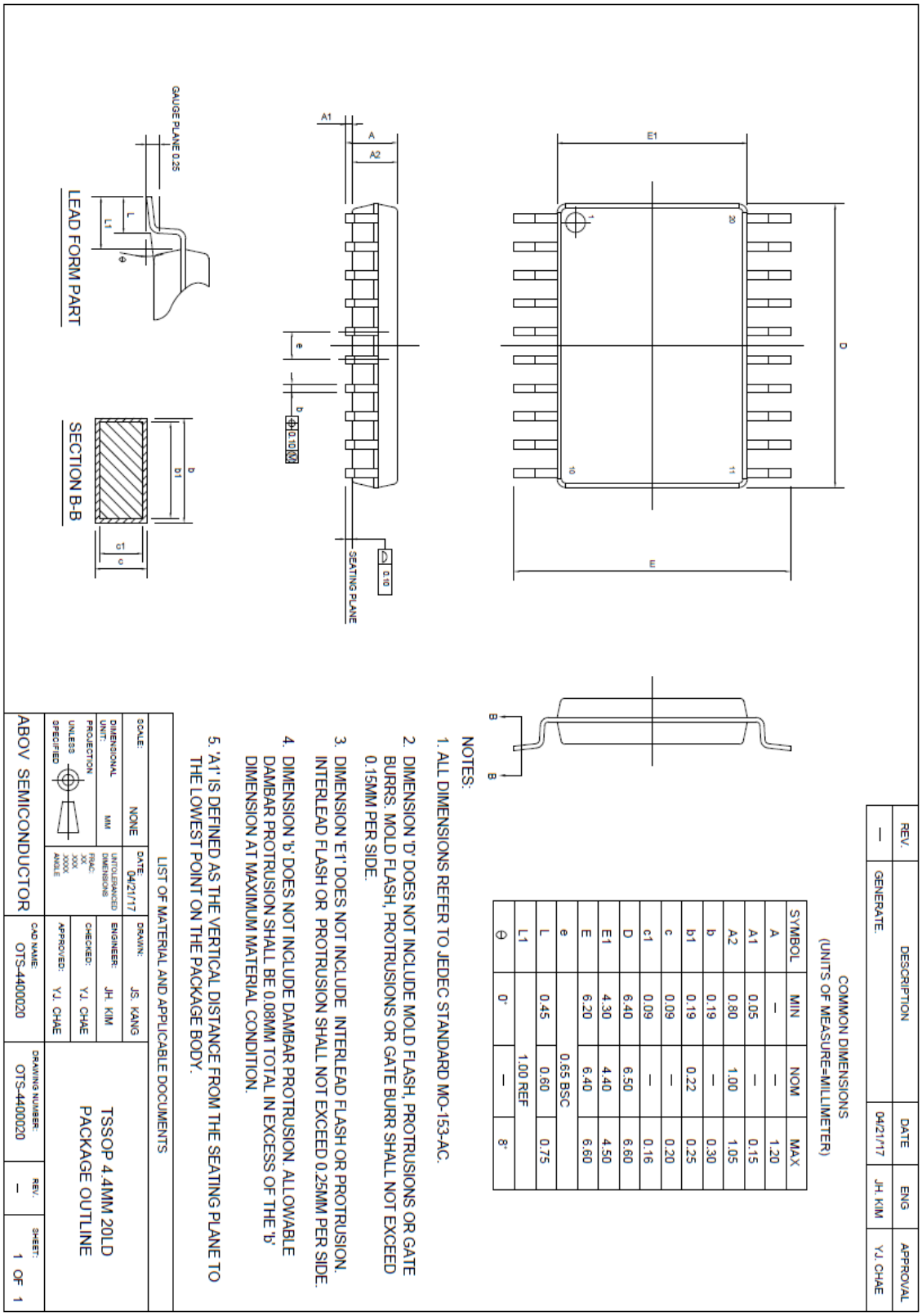


# 5. Package Information

## 5.1 20-TSSOP Package Information

20-TSSOP is a 20-pin, 4.4 x 6.5 mm Thin-Shrink Small-Outline Package.

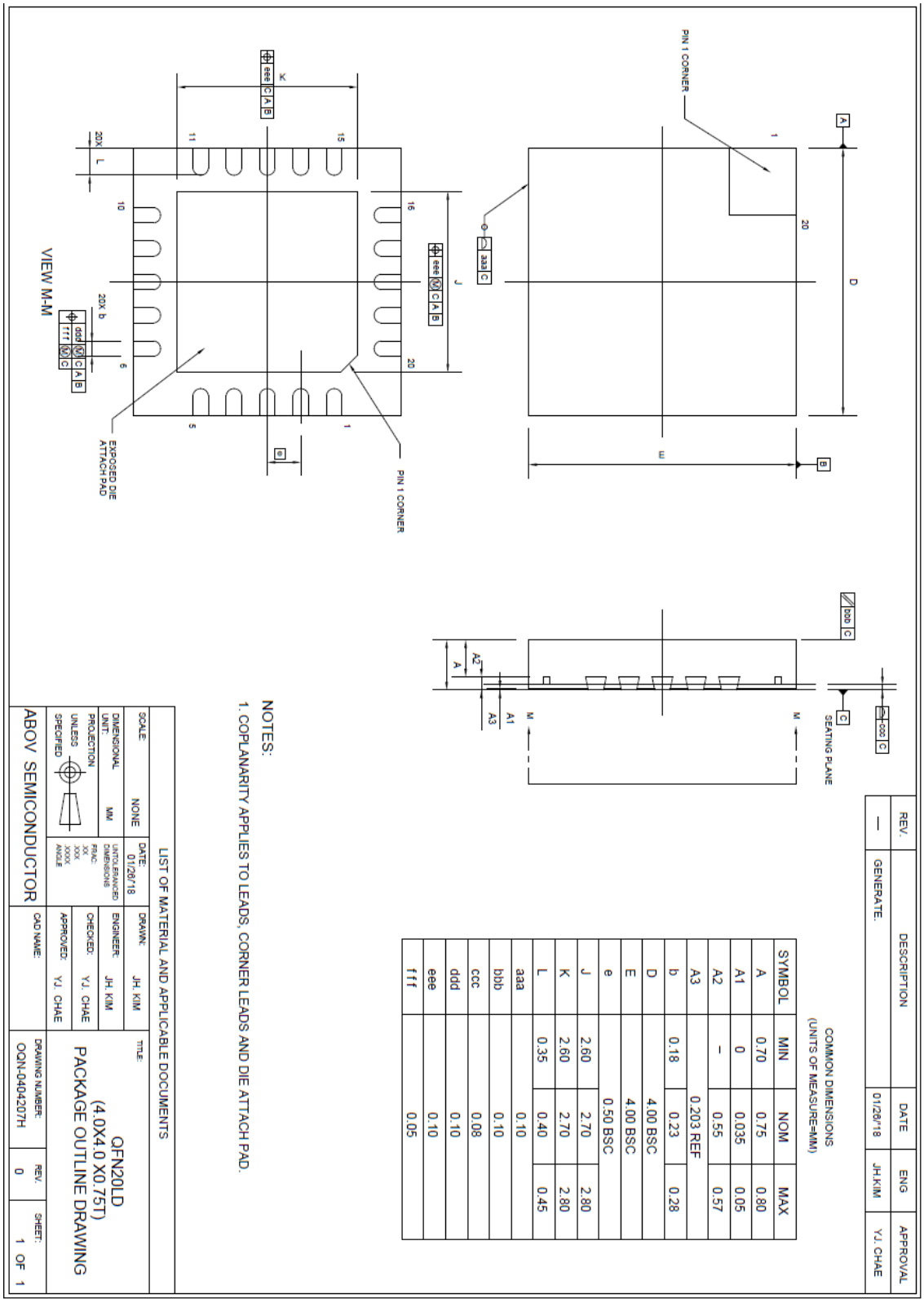
**Figure 63. 20-TSSOP Package Dimension**



## 5.2 20-QFN Package Information

20-QFN is a 20-pin, 4 x 4 mm Quad Flat No-lead package.

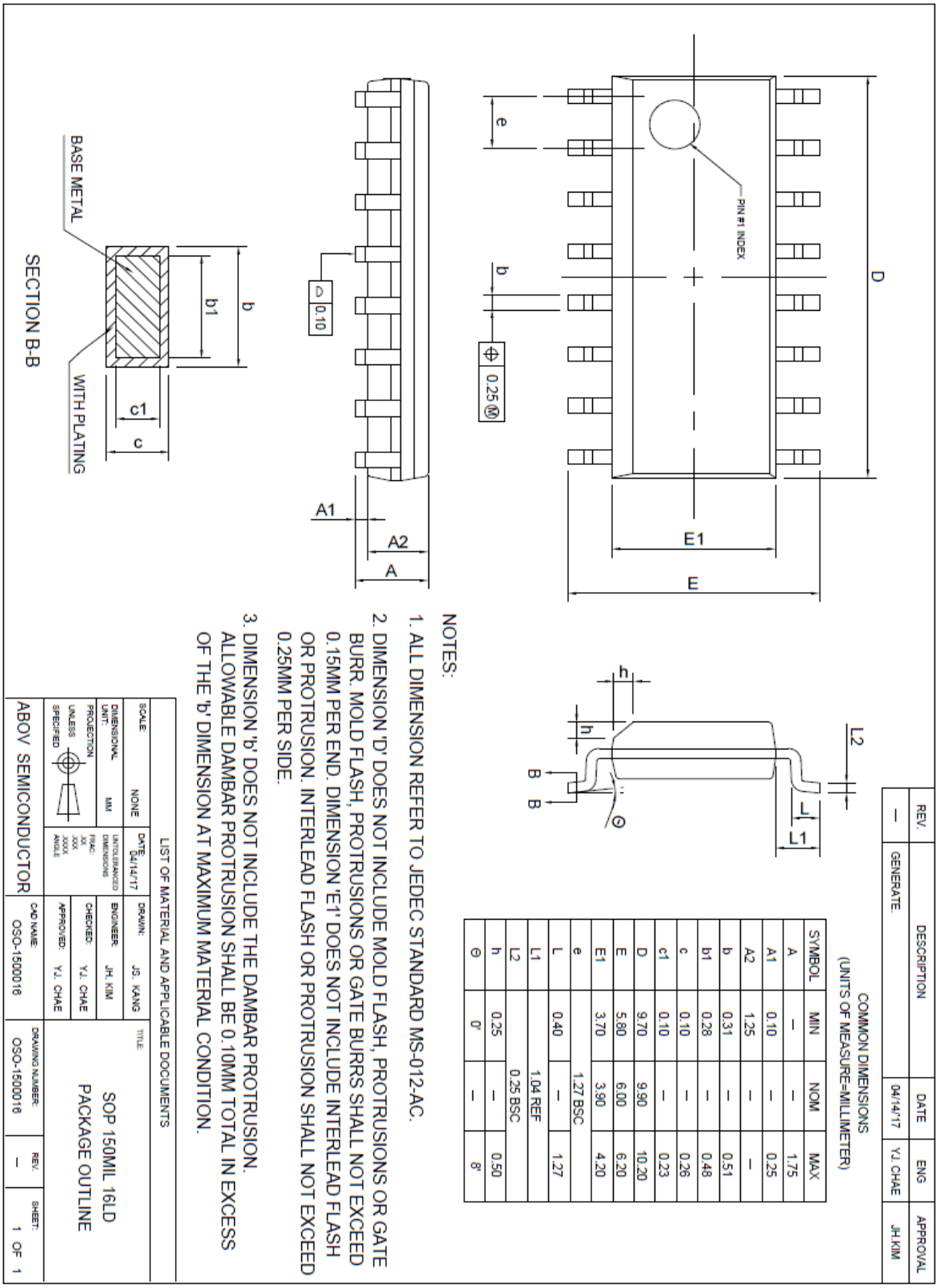
**Figure 64. 20-QFN Package Dimension**



## 5.3 16-SOPN Package Information

16-SOPN is a 16-pin, 3.9 x 9.9 mm Small Outline Package.

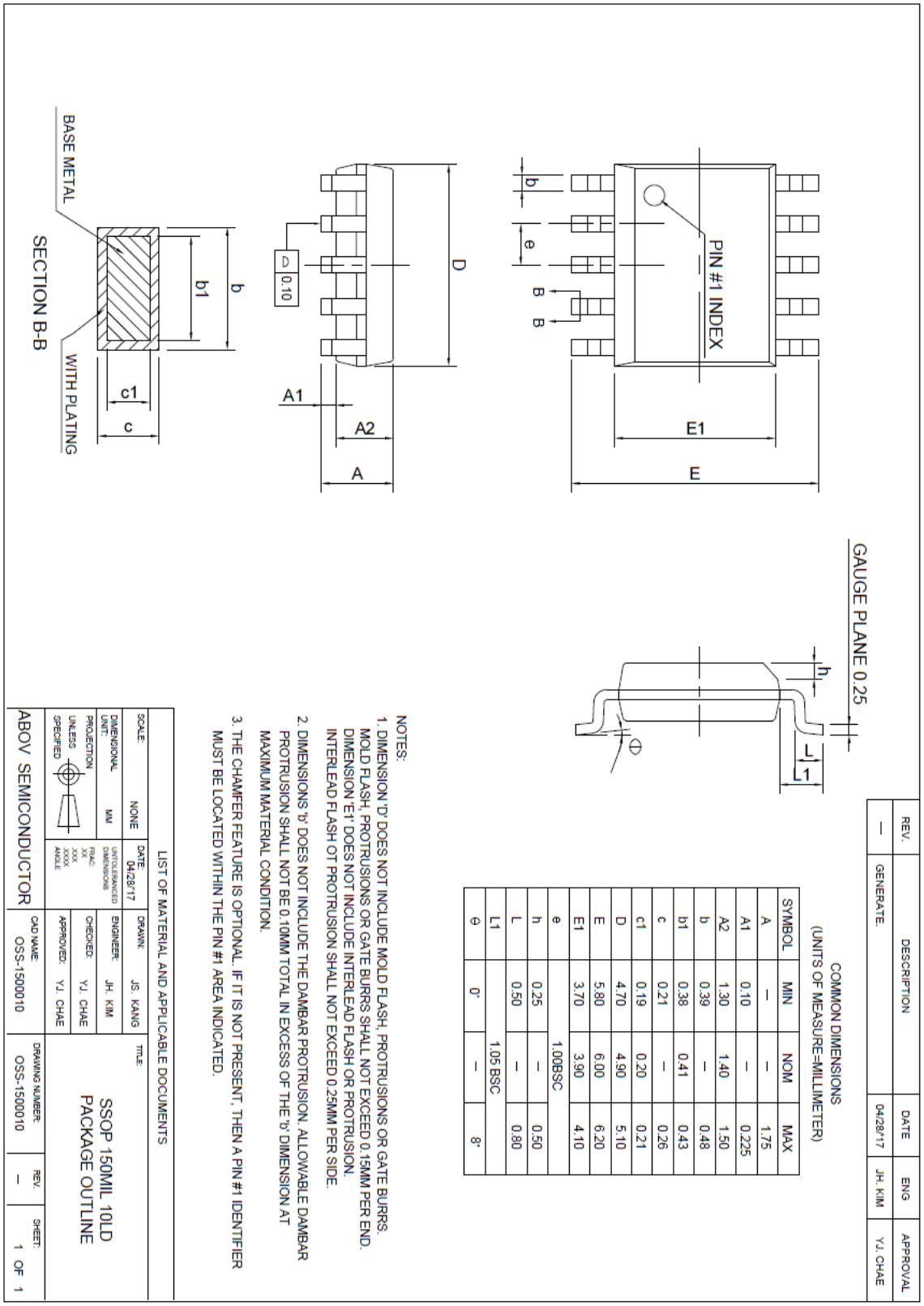
**Figure 65. 16-SOPN Package Dimension**



## 5.4 10-SSOP Package Information

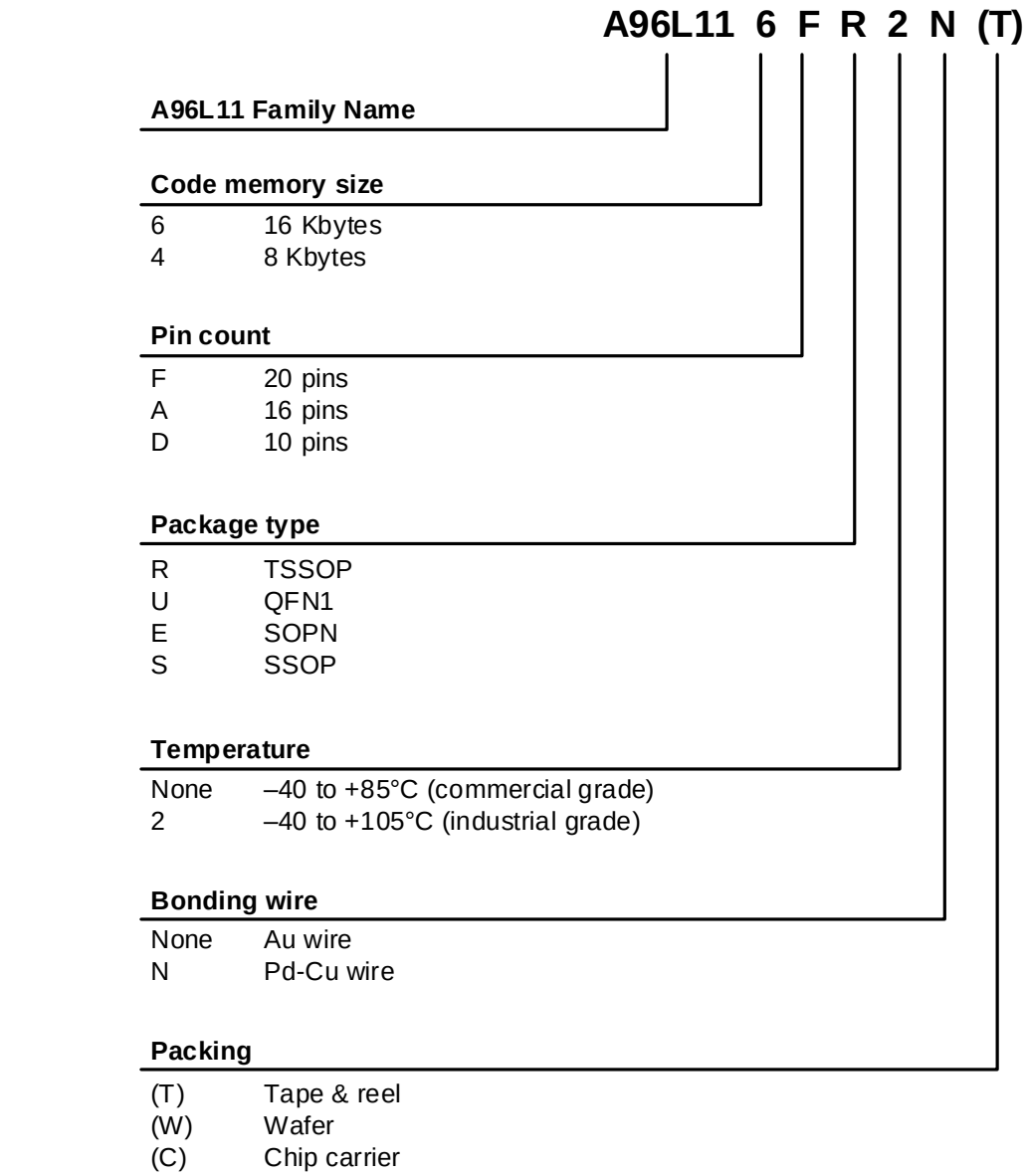
10-SSOP is a 10-pin, 3.9 x 4.9 mm Shrink Small Outline Package.

**Figure 66. 10-SSOP Package Dimension**



# 6. Ordering Information

**Figure 67. A96L116 Ordering Information**




**NOTE:**

1. For more information on any aspect of this device, please contact your nearest distributor or ABOV sales office.

# Revision History

| Date | Version | Description |
|---|---|---|
| Dec. 22, 2023 | 1.00 | First creation |
| Apr. 24, 2024 | 1.01 | Corrected typos and revised 20-QFN package dimensions. |
| Dec. 2, 2024 | 1.03 | Updated the disclaimer. |

**Korea**

**Regional Office, Seoul**
**R&D, Marketing & Sales**
8th Fl., 330, Yeongdong-daero,
Gangnam-gu, Seoul,
06177, Korea

Tel: +82-2-2193-2200
Fax: +82-2-508-6903
www.abovsemi.com

**HQ, Ochang**
**R&D, QA, and Test Center**
37, Gangni 1-gil, Ochang-eup,
Cheongwon-gun,
Chungcheongbuk-do,
28126, Korea

Tel: +82-43-219-5200
Fax: +82-43-217-3534
https://www.abovsemi.com/en/main.php

**Domestic Sales Manager**
Tel: +82-2-2193-2206
Fax: +82-2-508-6903
Email: sales_kr@abov.co.kr

**Global Sales Manager**
Tel: +82-2-2193-2281
Fax: +82-2-508-6903
Email: sales_gl@abov.co.kr

**China Sales Manager**
Tel: +86-755-8287-2205
Fax: +86-755-8287-2204
Email: sales_cn@abov.co.kr

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